E85: Digital Design and Computer Architecture

Problem Set 5

1) SystemVerilog to State Transition Diagram

   Do Exercise 4.24 from DDCA ARMed.

2) SystemVerilog Logic Design

   Design a serial (one bit at a time) two's complementer FSM with two inputs, Start and A, and one output, Q. A binary number of arbitrary length is provided to input A, starting with the least significant bit. The corresponding bit of the output appears at Q on the same cycle. Start is asserted for one cycle to initialize the FSM before the least significant bit is provided. You may find it helpful to try some cases by hand to figure out how the output should depend on the input. Express your design in behavioral SystemVerilog.

3) Priority Circuit

   An N-input lowest priority circuit has input $A_{N-1:0}$ and output $Y_{N-1:0}$. $Y_j = 1$ if $A_j = 1$ and $A_k = 0$ for all $k < j$. In other words, it asserts a bit in Y corresponding to the *least* significant bit asserted in A.

   Suppose each 2-input gate has a delay of 10 ps and an inverter has a delay of 5 ps. Design a 16-input lowest priority circuit with a propagation delay not exceeding 55 ps. Sketch a schematic for your circuit. If you are spending too much time on this problem, you may relax the delay requirement to 180 ps for partial credit.

4) Impact on society: Identify an item you use in your life that you know or could reasonably expect was primarily implemented by synthesizing hardware description language code onto a chip or FPGA (as opposed to mainly writing code for a microcontroller, building an analog electronic or mechanical device, etc.) Why was HDL an appropriate design methodology for the item?

5) How long did you spend on this problem set? This will not count toward your grade but will help calibrate the workload.