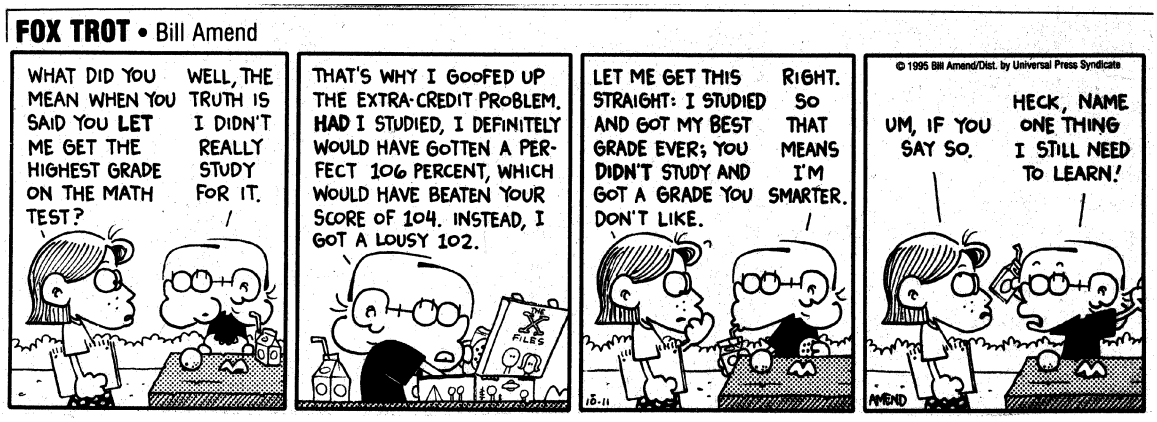
Introduction to Computer Engineering (E114)

Harris Spring 2000

Midterm



This is an open book, open notes quiz. You may use any resources except other *homo sapiens*.

Along side each question, the number of points is written in brackets. The entire exam is worth 50 points. Plan your time accordingly. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. Show your work for partial credit.

Name: _____

Section: ___ 1: 9-10

___ 2: 10-11

Do Not Write Below This Point

Pages 2-3: _____ /16

Page 4: _____ /7

Page 5: _____ /8

Page 6: _____ /11

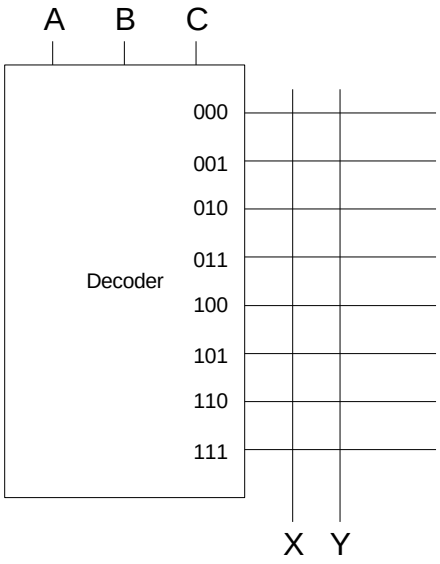
Page 7: _____ /8

Total: _____ /50

Consider the implementing the following two Boolean functions:

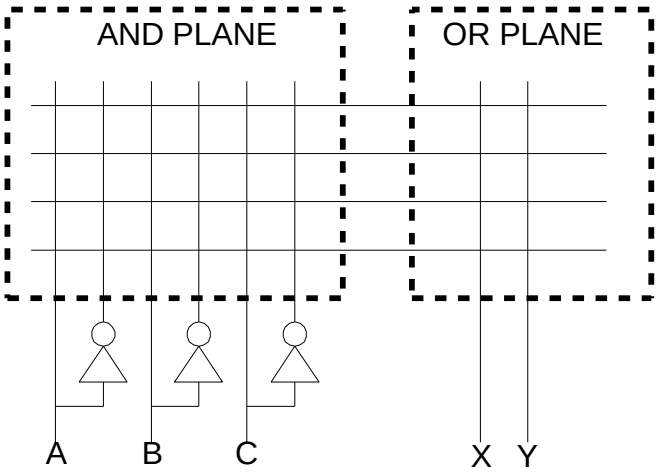
$$X = A \bullet B + C \bullet \overline{B}$$
$$Y = \overline{A} \bullet B \bullet \overline{C} + A \bullet B$$

1. [3] Complete a dot diagram for a 8-word x 2-bit ROM.



ROM Dot Diagram

2. [3] Complete a dot diagram for a PLA. Use no more minterms than necessary.



PLA Dot Diagram

3. [4] Use only two four-input multiplexers (and no other gates). Assume true and complementary inputs are available.

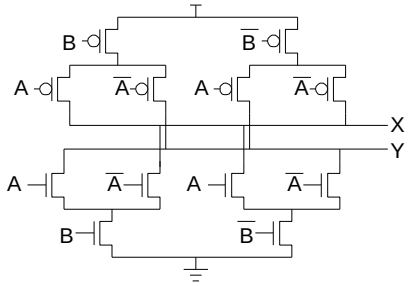
Multiplexer Design

4. [6] Use AND, OR, and NOT gates. Provide a design with no hazards and explain how you know your design has no hazards.

Gate Design

Explanation

5. [3] Complete a truth table for the following transistor-level circuit:



A	B	X	Y
0	0		
0	1		
1	0		
1	1		

Truth Table

6. [4] Sketch a 3-input OR gate using MOS transistors.

Transistor-Level Design

Write -6.375 as a:

7. [2] 8 bit sign/magnitude number with 4 integer bits and 4 fraction bits

Sign/Magnitude Number _____

8. [3] 8-bit 2's complement number with 5 integer bits and 3 fraction bits

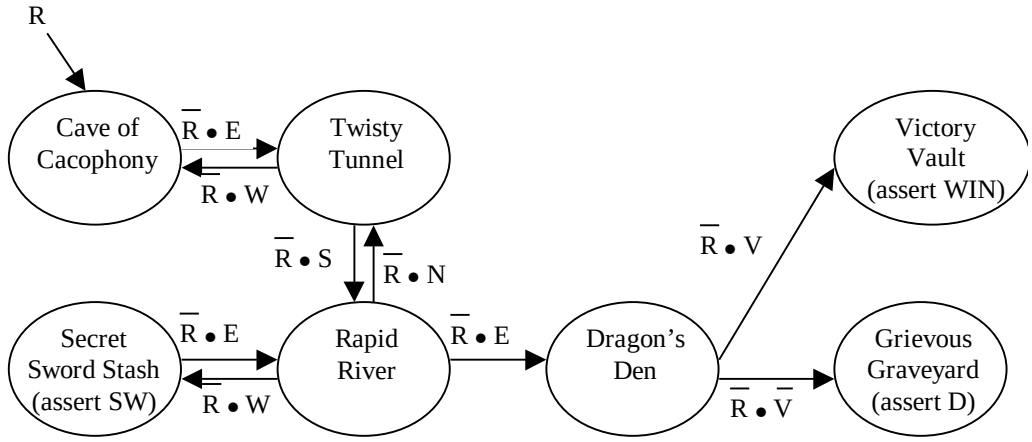
2's Complement Number _____

9. [3] IEEE single-precision floating-point number

IEEE Floating-Point Number _____

According to the Extra Credit portion of Lab 3 that nobody did, by heading north from the Twisty Tunnel, one can reach the Harvey Mudd campus. In this problem, you will extend the adventure game Room FSM to include Platt directly north from the Twisty Tunnel. To do this, modify the logic from the Lab 3 solutions shown below.

10. [3] Add a state for Platt to the State Transition Diagram below. Be sure to label the transitions to and from the state.



11. [4] Using the following state encodings, extend the state table below to include your new state.

State	N	S	E	W	R	V	Next State	SW	D	WIN
X	X	X	X	X	1	X	00000001	0	0	0
00000001	X	X	1	X	0	X	00000010	0	0	0
00000010	X	X	X	1	0	X	00000001	0	0	0
00000010	X	1	X	X	0	X	00000100	0	0	0
00000100	1	X	X	X	0	X	00000010	0	0	0
00000100	X	X	X	1	0	X	00001000	1	0	0
00000100	X	X	1	X	0	X	00010000	0	0	0
00001000	X	X	1	X	0	X	00000100	0	0	0
00010000	X	X	X	X	0	0	00100000	0	1	0
00010000	X	X	X	X	0	1	01000000	0	0	1

State Encodings
CC = 00000001
TT = 00000010
RR = 00000100
SS = 00001000
DD = 00010000
GG = 00100000
VV = 01000000
PLATT = 10000000

12. [4] The Boolean equations for the Lab 3 Room FSM are listed below. Modify and add equations to incorporate your changes from the previous problem.

$S1' = R + S2 \bullet W$

$S2' = S1 \bullet E \bullet \overline{R} + S3 \bullet N \bullet \overline{R}$

$S3' = S2 \bullet S \bullet \overline{R} + S4 \bullet E \bullet \overline{R}$

$S4' = S3 \bullet W \bullet \overline{R}$

$S5' = S3 \bullet E \bullet \overline{R}$

$S6' = S5 \bullet \overline{V} \bullet \overline{R}$

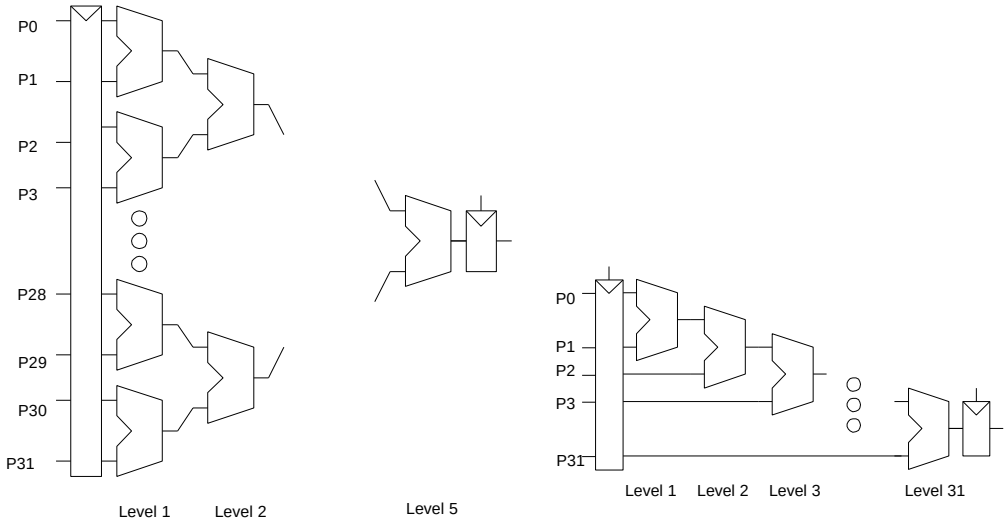
$S7' = S5 \bullet V \bullet \overline{R}$

$SW = S4'$

$D = S6'$

$WIN = S7'$

Ben Bitdiddle is designing a 32x32-bit multiplier. He needs to sum 32 64-bit partial products P0…P31 to form a 64-bit result. He is considering two designs for the adder, both built from 2-input 64-bit adders. Ben is working in a 0.18 micron CMOS process with a 64-bit adder propagation delay of 1000 ps and a contamination delay of 50 ps. The flip-flops in his process have a setup time of 120 ps, a hold time of 30 ps, and clock-to-Q propagation delays of 80 ps and contamination delays of 40 ps.



Design I: Tree Design II: Linear Array

13. [4] If there is no clock skew, what is the minimum clock period at which each design will operate reliably? Show your reasoning.

Design I Clock Period _____ Design II Clock Period _____

14. [4] How much clock skew could each design experience before suffering a hold time violation? Show your reasoning.

Design I Skew _____ Design II Skew _____