Digital Electronics & Computer Engineering (E85)
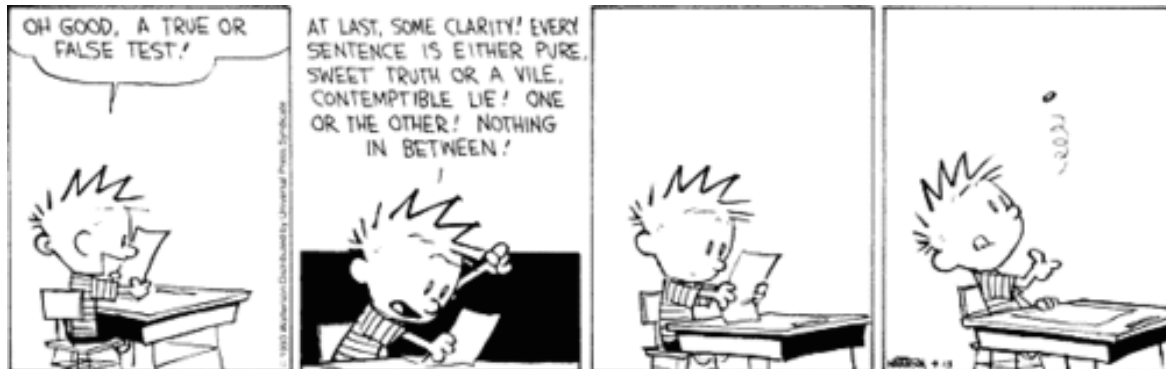
Harris   Spring 2019

Midterm

This is a closed-book take-home exam. Electronic devices including calculators are not allowed. You are permitted one side of one 8.5x11" sheet of paper with notes.

You are bound by the HMC Honor Code while taking this exam.

This is a 75-minute exam, but everyone in the class is granted extra time up to 120 contiguous minutes total so you should not feel time pressure if you have prepared adequately. You are responsible for monitoring your time.

Return the exam under Prof. Harris' door no later than Wednesday 3/6 at 11 am.

Along side each question, the number of points is written in brackets. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Show your work for partial credit.
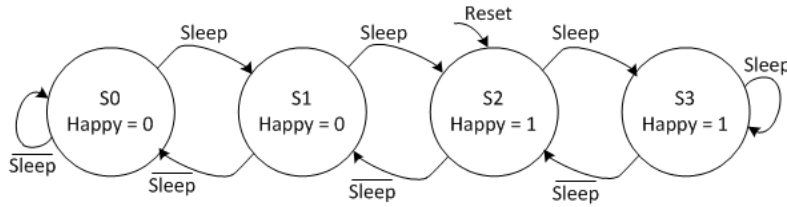
Name: _____

Score

Page 2:	_____	/ 4
Page 3:	_____	/ 8
Page 4:	_____	/ 9
Page 5:	_____	/ 9
Total:	_____	**/ 30**

Write -9_{10} as a 6-bit 2's complement binary number.

_____ [1]

Sketch a CMOS transistor-level implementation of a 3-input OR gate. [3]

Consider the following FSM state transition diagram.   The FSM has one input, Sleep, and one output, Happy. The clock period is 24 hours. Use a binary encoding with S0 = 00, S1 = 01, S2 = 10, S3=11.

Reset

Sleep   Sleep   Sleep   Sleep

S0   S1   S2   S3
Happy = 0   Happy = 0   Happy = 1   Happy = 1
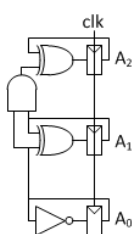
Sleep

Sleep   Sleep   Sleep

Write truth tables for the next state and output logic. [3]

Write minimal sum of products equations for the next state and output. [2]

Sketch a circuit for the FSM. [3]

Consider the following circuit and element delays.

Cell	Propagation Delay (ps)	Contamination Delay (ps)	Setup Time (ps)	Hold Time (ps)
NOT	7	4		
NAND (2-input)	8	6		
AND (2-input)	12	10		
XOR (2-input	15	11		
Flop	20	14	9	5

Is this circuit combinational or sequential?

Combinational   Sequential   [1]

Write a Verilog module describing the circuit. [3]

```
module midterm(input  logic clk,
           output logic [2:0] a);
```



```
endmodule
```

What is the minimum clock period for which the circuit will operate correction with no clock skew?

_____[3]

What is the maximum clock skew for which the circuit will operate correctly, if the clock period is long?

_____[2]

Consider the following circuit. Assume that each gate has
the propagation delay listed in the previous problem.
Assume that each gate has a capacitance of 3 fF on each
input pin and that other capacitances are negligible. Each
gate draws a leakage current of 10 nA from its power supply
(VDD) while idle. The power supply voltage is 2 V.

A
B
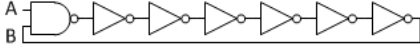
When A = 1, what frequency will node B oscillate at?

_____[3]

When A = 1, approximately how much power will the circuit
draw from VDD?

_____[3]

When A = 0, how much power will the circuit draw from VDD?

_____[3]