# Digital Electronics \& Computer Engineering (E85) 

This is a closed-book take-home exam. Electronic devices including calculators are not allowed. You are permitted one $8.5 \times 11$ " sheet of paper with notes.

You are bound by the HMC Honor Code while taking this exam.
The exam is intended to be doable in 75 minutes, but everyone in the class is granted extra time up to 180 contiguous minutes so you should not feel time pressure if you have prepared adequately.

Return the exam under Prof. Harris' door no later than Friday $3 / 3$ at midnight.
Along side each question, the number of points is written in brackets. The entire exam is worth 30 points. Plan your time accordingly. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. Show your work for partial credit.

Name: $\qquad$

## Do Not Write Below This Point

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Total: $\qquad$ / 30
[3] What are the largest and smallest 5-bit numbers in each of the following number systems?

|  | Largest | Smallest |
| :--- | :--- | :--- |
| Unsigned |  |  |
| Sign-Magnitude |  |  |
| Two's Complement |  |  |

[4] Assign $\mathrm{V}_{\mathrm{IL}}, \mathrm{V}_{\mathrm{IH}}, \mathrm{V}_{\mathrm{OL}}$, and $\mathrm{V}_{\mathrm{OH}}$ to maximize the smallest of the two noise margins. What noise margins do you achieve? What is the logic function?


## Logic Function:

$V_{\text {IL }}$ $\qquad$ $\mathbf{V I H}_{\text {IH }}$ $\qquad$ $V_{\text {OL }}$ $\qquad$ $\mathrm{VOH}_{\mathrm{OH}}$ $\qquad$
$\mathbf{N M}_{\mathbf{L}}$ $\qquad$ $\mathbf{N M}_{\mathbf{H}}$ $\qquad$

The Xilinx Spartan 3 FPGA has propagation and contamination delays of 0.61 and 0.30 ns , respectively, for each lookup table (LUT). It also contains flip-flops with propagation and contamination delays of 0.72 and 0.50 ns , and setup and hold times of 0.53 and 0 ns , respectively.
[3] If you are building a system that needs to run at 200 MHz , how many consecutive LUTs can you place between two flip-flops? Assume that there is no clock skew and no delay through wires between LUTs.

## Consecutive LUTs:

$\qquad$
[3] Suppose that all paths between flip-flops pass through at least one LUT. How much clock skew can the FPGA withstand without violating a hold time?

## Clock Skew:

$\qquad$

Gray codes have a useful property in that consecutive numbers differ in only a single bit position. The table below lists a 3-bit Gray code representing the numbers from 0 to 7 . Design a Gray code counter that steps through the 3-bit values in this sequence. The counter should take clock and reset inputs and produce a 3-bit output.

| Number | Gray code |  |  |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 1 |
| 3 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0 |
| 5 | 1 | 1 | 1 |
| 6 | 1 | 0 | 1 |
| 7 | 1 | 0 | 0 |

[4] Sketch a schematic for the counter.
[4] Write graceful SystemVerilog code for your counter.

```
module midterm(input logic
    clk, reset,
    output logic [2:0] q);
```

[3] Find a minimal sum-of-products expression for the function described by the truth table below. Take advantage of the don't care entries.

| $\boldsymbol{A}$ | $\boldsymbol{B}$ | $\boldsymbol{C}$ | $\boldsymbol{D}$ | Y |
| :--- | :--- | :--- | :--- | :--- |
| $\mathbf{0}$ | 0 | 0 | 0 | X |
| $\mathbf{0}$ | 0 | 0 | 1 | X |
| $\mathbf{0}$ | 0 | 1 | 0 | X |
| $\mathbf{0}$ | 0 | 1 | 1 | 0 |
| $\mathbf{0}$ | 1 | 0 | 0 | 0 |
| $\mathbf{0}$ | 1 | 0 | 1 | X |
| $\mathbf{0}$ | 1 | 1 | 0 | 0 |
| $\mathbf{0}$ | 1 | 1 | 1 | X |
| $\mathbf{1}$ | 0 | 0 | 0 | 1 |
| $\mathbf{1}$ | 0 | 0 | 1 | 0 |
| $\mathbf{1}$ | 0 | 1 | 0 | X |
| $\mathbf{1}$ | 0 | 1 | 1 | 1 |
| $\mathbf{1}$ | 1 | 0 | 0 | 1 |
| $\mathbf{1}$ | 1 | 0 | 1 | 1 |
| $\mathbf{1}$ | 1 | 1 | 0 | X |
| $\mathbf{1}$ | 1 | 1 | 1 | 1 |

$\qquad$
[2] Sketch an implementation using only NAND gates. Use as few as possible.

You are walking down the hallway when you run into your lab partner walking in the other direction. The two of you first step one way and are still in each other's path. You then both step the other way. You then both wait a bit, hoping the other person will step aside, but then both unfortunately step back the other way again simultaneously. You can model this situation as a metastable point and apply the same theory that has been applied to synchronizers. Suppose you create a mathematical model of this situation in which you both begin the encounter in a metastable state. The probability that you remain in this state after $t$ seconds is $e^{-\frac{t}{\tau}}$. $\tau$ indicates your response rate; today your brain is addled by lack of sleep and has $\tau=20$ seconds.
[2] Give an expression for how long it will be until you have $99 \%$ certainty that you will have resolved from metastability (i.e. figured out how to pass each other.)

Time for $\mathbf{9 9 \%}$ chance of resolution: $\qquad$
[2] You are not only sleepy, but also ravenously hungry. In fact, you will starve to death if you don't get going to the dining hall within 3 minutes. Give an expression for the probability that you will live to build circuits another day.

## Probability of survival:

