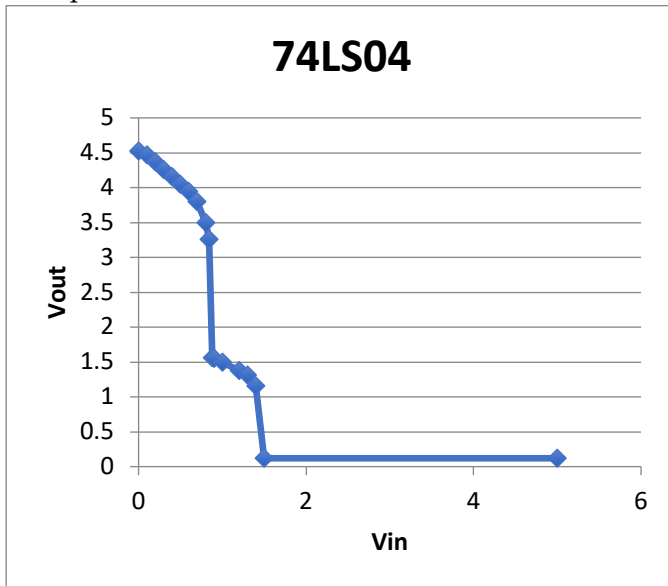


E85: Digital Design and Computer Engineering

Problem Set 2

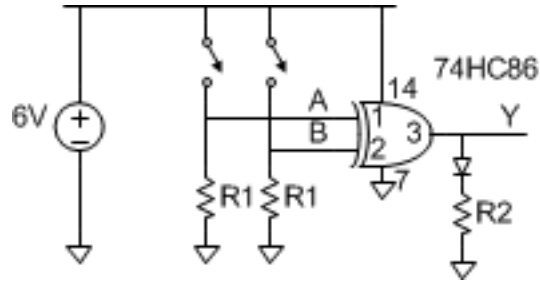
- 1) The voltage transfer characteristics below are measured for a 74LS04 operating at 5V. Determine V_{IL} , V_{IH} , V_{OL} , V_{OH} , and the high and low noise margins. Compare your results to the 74LS specification in Table eA.2 of the textbook. Are they within the specifications?



- 2) Referring to the logic level specifications in Tables eA.2 and eA.3 of the textbook:
- What could go wrong if a 74LS04 inverter drives a 74HC08 AND gate?
 - In light of your answer to Part (a), why does the HCT family exist?
 - Can a 3.3V 74LVC32 gate reliably drive a 5V 74HC00?
 - Can a 3.3V 74LVC32 gate reliably drive a 5V 74HCT00?
 - Can a 74HC00 reliably drive a 3.3V 74LVC32?
- 3) Power consumption

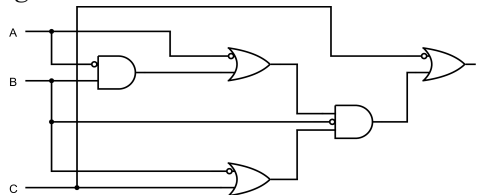
Hint: refer to the Switches and Diodes Tutorial at the end of this problem set if you are unfamiliar with electrical calculations for these components.

The following circuit turns on an LED when you press one button or another but not both. The circuit operates directly from a 6V Ni-MH battery with a 280 mA-hr energy capacity. The data sheet for the 74HC86 XOR gate is attached to the end of this problem set. The circuit is in a hot enclosure that might reach 85 °C. You push the buttons slowly enough that dynamic power consumption is negligible.



- What is the quiescent power consumption of the XOR gate in the hot enclosure?
- What value of $R1$ should you use to minimize power consumption when the button is pressed, while still providing a valid logic level at the input of the XOR when the button is not pressed, considering input leakage current?
- What value of $R2$ should you use to maximize the brightness of the LED without exceeding the I_{OH} output current specification? Assume that the LED has a 2 V drop across it when ON.
- Suppose that both buttons are pressed 99.9% of the time and that a single button is pressed the remainder of the time. What is the average power consumption? Be sure to account for quiescent consumption of the gate, power dissipated in the input resistors, and power delivered to the load.
- How long will the battery last?
- If you were willing to violate I_{OH} , what is the minimum value of $R2$ that you could use without risking damage to the 74HC86?

4) Consider the following logic circuit:



- Write the Boolean equation performed by the above diagram.
 - Simplify the equation using Boolean identities.
 - Write a truth table describing the circuit.
 - Show how to implement the simplified function with logic gates.
 - Show how to implement the function in SystemVerilog.
 - Sketch a transistor-level implementation of the simplified function using CMOS transistors.
- 5) Impact on Society: Integrated circuits have been following Moore's Law since 1965, with cost per transistor reducing approximately 30% per year. This progress is slowing as nanometer lithography is becoming extremely expensive. Supposing cost reduction grinds to a halt by 2022, write a thoughtful paragraph predicting a significant impact on society caused by the end of Moore's Law.

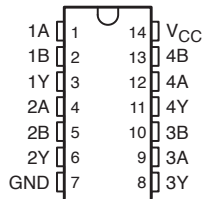
How long did you spend on this problem set? This will not count toward your grade but will help calibrate the workload.

SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

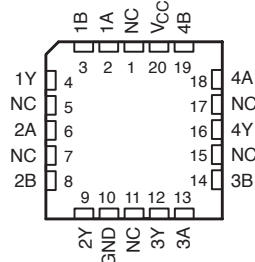
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- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 20- μ A Max I_{CC}
- Typical $t_{pd} = 10$ ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- True Logic

SN54HC86 . . . J OR W PACKAGE
SN74HC86 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube of 25	SN74HC86N	SN74HC86N
	SOIC – D	Tube of 50	SN74HC86D	HC86
		Reel of 2500	SN74HC86DR	
		Reel of 250	SN74HC86DT	
	SOP – NS	Reel of 2000	SN74HC86NSR	HC86
	TSSOP – PW	Tube of 90	SN74HC86PW	HC86
Reel of 2000		SN74HC86PWR		
Reel of 250		SN74HC86PWT		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC86J	SNJ54HC86J
	CFP – W	Tube of 150	SNJ54HC86W	SNJ54HC86W
	LCCC – FK	Tube of 55	SNJ54HC86FK	SNJ54HC86FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to ML-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

1

**SN54HC86, SN74HC86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES**

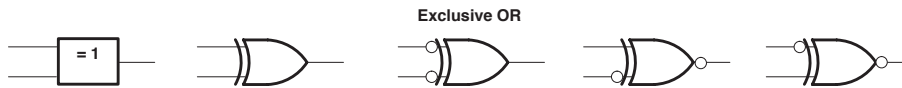
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FUNCTION TABLE
(each gate)

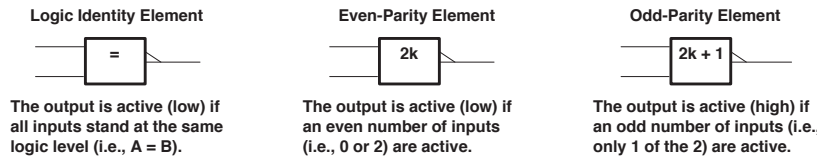
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These are five equivalent exclusive-OR symbols valid for an 'HC86 gate in positive logic; negation may be shown at any two ports.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
N package	80°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54HC86, SN74HC86 QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

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recommended operating conditions (see Note 3)

		SN54HC86			SN74HC86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	2	5	6	2	5	6	V
V _{IH}	High-level input voltage	V _{CC} = 2 V		1.5	1.5		V	
		V _{CC} = 4.5 V		3.15	3.15			
		V _{CC} = 6 V		4.2	4.2			
V _{IL}	Low-level input voltage	V _{CC} = 2 V			0.5		V	
		V _{CC} = 4.5 V			1.35			
		V _{CC} = 6 V			1.8			
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
Δt/Δv	Input transition rise/fall time	V _{CC} = 2 V		1000		1000		ns
		V _{CC} = 4.5 V		500		500		
		V _{CC} = 6 V		400		400		
T _A	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V _{CC}	T _A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V	1.9	1.998		1.9	1.9	V		
			4.5 V	4.4	4.499		4.4	4.4			
			6 V	5.9	5.999		5.9	5.9			
		I _{OH} = -4 mA	4.5 V	3.98	4.3		3.7	3.84			
		I _{OH} = -5.2 mA	6 V	5.48	5.8		5.2	5.34			
V _{OL}	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V		0.002	0.1		0.1	V		
			4.5 V		0.001	0.1		0.1			
			6 V		0.001	0.1		0.1			
		I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I _{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0		6 V		±0.1	±100		±1000	±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0		6 V			2		40	20	μA	
C _i			2 V to 6 V		3	10		10	10	pF	



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3

Switches and Diodes Tutorial

A single-pole single-throw (SPST) switch or button is either open or closed, blocking or allowing current to flow, respectively. To produce a digital logic level, the switch is normally placed in series with a resistor, as shown below.



Assume that the switch has negligible internal resistance. When the switch is closed, the output Y is pulled up to V_{DD} through the switch. The circuit dissipates $P = V_{DD}^2/R$ across the resistor. When the switch is open, the output Y is pulled down close to 0 through the resistor. If the load draws some current I_{load} (e.g. the input leakage current of a gate attached to Y), it will cause a voltage drop $V_Y = I_{load} * R$ across the resistor instead of getting all the way down to 0.

The resistor should be chosen according to the Goldilocks principle: not too big, not too small, but just right. If the resistor is too large, V_Y won't fall low enough. If the resistor is too small, the circuit dissipates excessive and wasteful power (or might even melt down). As a practical matter, this often means the resistor is selected in the 1-10 $K\Omega$ range such that the power is small and leakage causes a negligible disturbance to the output voltage. However, if extremely low power operation is needed, a larger resistor would be appropriate and the leakage must be considered more carefully so that the output voltage remains a valid low logic level.

A light emitting diode (LED) can be approximated as OFF when the voltage across the diode is less than some voltage V_D and ON when the voltage is greater than V_D . V_D varies from about 1.7 to 2.3 V depending on the color of the diode and the ambient temperature, but 2.0 V is a reasonable average for rough calculations. When the diode is off, it draws negligible current. When it is ON, it draws as much current I_D as it can, and the brightness is proportional to the current. However, if the current is too great, the diode or the device sourcing the current will burn out. Hence, diodes are normally used with current-limiting resistors, as shown above. Ordinary small diodes typically are visible in indoor lighting when they carry more than 1 mA and glow nicely at 5-10 mA. Ultrabright LEDs might draw 100 mA or more.

The voltage across the resistor is $V_{in} - V_D$ because of the voltage drop across the diode, and it is also $R * I_D$ because the current flowing through the diode also flows through the resistor. Equating these two, we find $R = (V_{in} - V_D)/I_D$. If R is too large, the diode will be too dim. If R is too small, the diode will burn out or draw too much current from the component driving V_{in} . Hence, resistors in the low hundreds of ohms are common in digital circuits driving LEDs.

A datasheet lists recommended operating conditions and absolute maximum ratings. The component will operate correctly within the recommended operating conditions. It is not guaranteed to be functional near the absolute maximums, but will not take permanent damage unless the maximums are exceeded.

Current always flows from high to low. Thus output current I_O flows out of the chip when the output is high, and into the chip when the output is low, and therefore has opposite signs in these two situations. The sign of the current is not very interesting; the magnitude is most important.

I_{CC} is the current flowing into the V_{CC} pin when the chip is quiescent. I_I is the input leakage current flowing into an input pin. V_{OL} and V_{OH} are often reported for a particular I_O output current. These logic levels are not guaranteed if the output current exceeds the indicated value.