E85 Digital Design & Computer Engineering

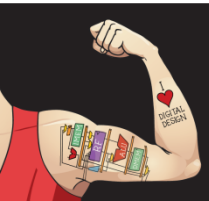
Lecture 1:

Logic Gates & Analog Behavior of Digital Systems

HARVEY MUDD COLLEGE

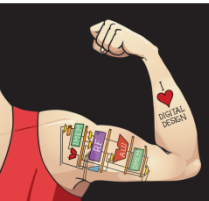
Lecture 1

- **Logic Gates**
- **Verilog**
- **Logic Levels**
- **CMOS Transistors**
- **Power Consumption**
- **Datasheets**



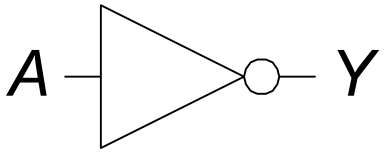
Logic Gates

- **Perform logic functions:**
  - inversion (NOT), AND, OR, NAND, NOR, etc.
- **Single-input:**
  - NOT gate, buffer
- **Two-input:**
  - AND, OR, XOR, NAND, NOR, XNOR
- **Multiple-input**



Single-Input Logic Gates

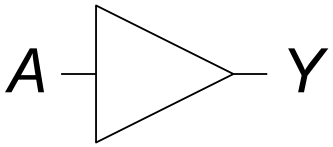
NOT



$Y = \overline{A}$

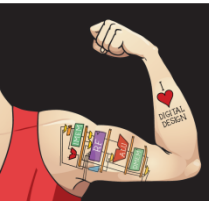
A	Y
0	
1	

BUF



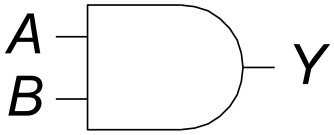
$Y = A$

A	Y
0	
1	



Two-Input Logic Gates

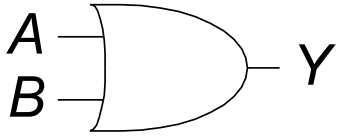
AND



$Y = AB$

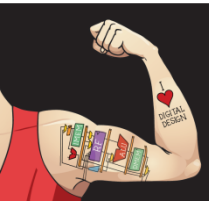
A	B	Y
0	0	
0	1	
1	0	
1	1	

OR



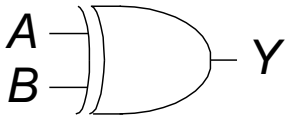
$Y = A + B$

A	B	Y
0	0	
0	1	
1	0	
1	1	



More Two-Input Logic Gates

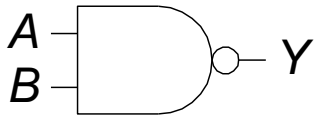
XOR



$Y = A \oplus B$

A	B	Y
0	0	
0	1	
1	0	
1	1	

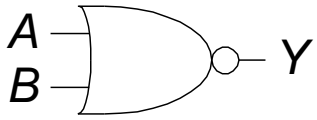
NAND



$Y = \overline{AB}$

A	B	Y
0	0	
0	1	
1	0	
1	1	

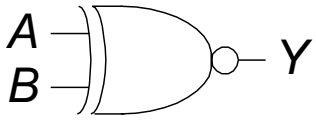
NOR



$Y = \overline{A + B}$

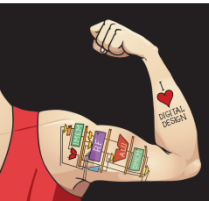
A	B	Y
0	0	
0	1	
1	0	
1	1	

XNOR



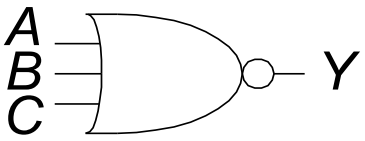
$Y = \overline{A \oplus B}$

A	B	Y
0	0	
0	1	
1	0	
1	1	



Multiple-Input Logic Gates

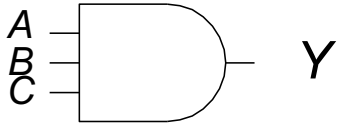
NOR3



$Y = \overline{A+B+C}$

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

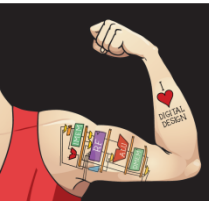
AND3



$Y = ABC$

A	B	C	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

- Multi-input XOR: Odd parity (true if odd number of inputs are true)



SystemVerilog Description

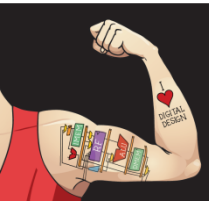
```
module gates(input  logic a, b, c,
             output logic y1, y2, y3, y4, y5);

  not  g1(y1, a);
  and  g2(y2, a, b);
  or   g3(y3, a, b, c);
  nand g4(y4, b, c);
  xor  g5(y5, a, c);
endmodule
```

- Multi-input XOR: Odd parity

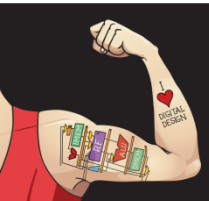
Logic Levels

- Discrete voltages represent 1 and 0
- For example:
  - 0 = *ground* (GND) or 0 volts
  - 1 = V_{DD} or 5 volts
- What about 4.99 volts? Is that a 0 or a 1?
- What about 3.2 volts?



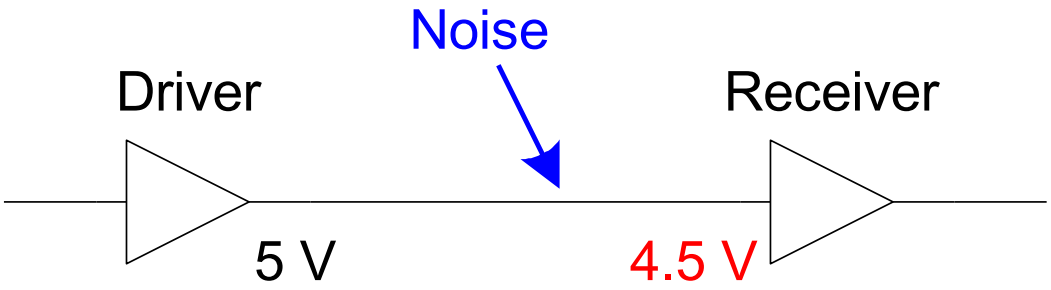
Logic Levels

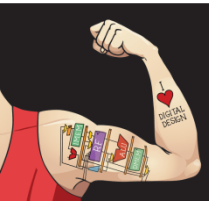
- *Range* of voltages for 1 and 0
- Different ranges for inputs and outputs to allow for *noise*



What is Noise?

- **Anything that degrades the signal**
  - E.g., resistance, power supply noise, coupling to neighboring wires, etc.
- **Example:** a gate (driver) outputs 5 V but, because of resistance in a long wire, receiver gets 4.5 V

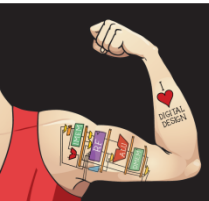




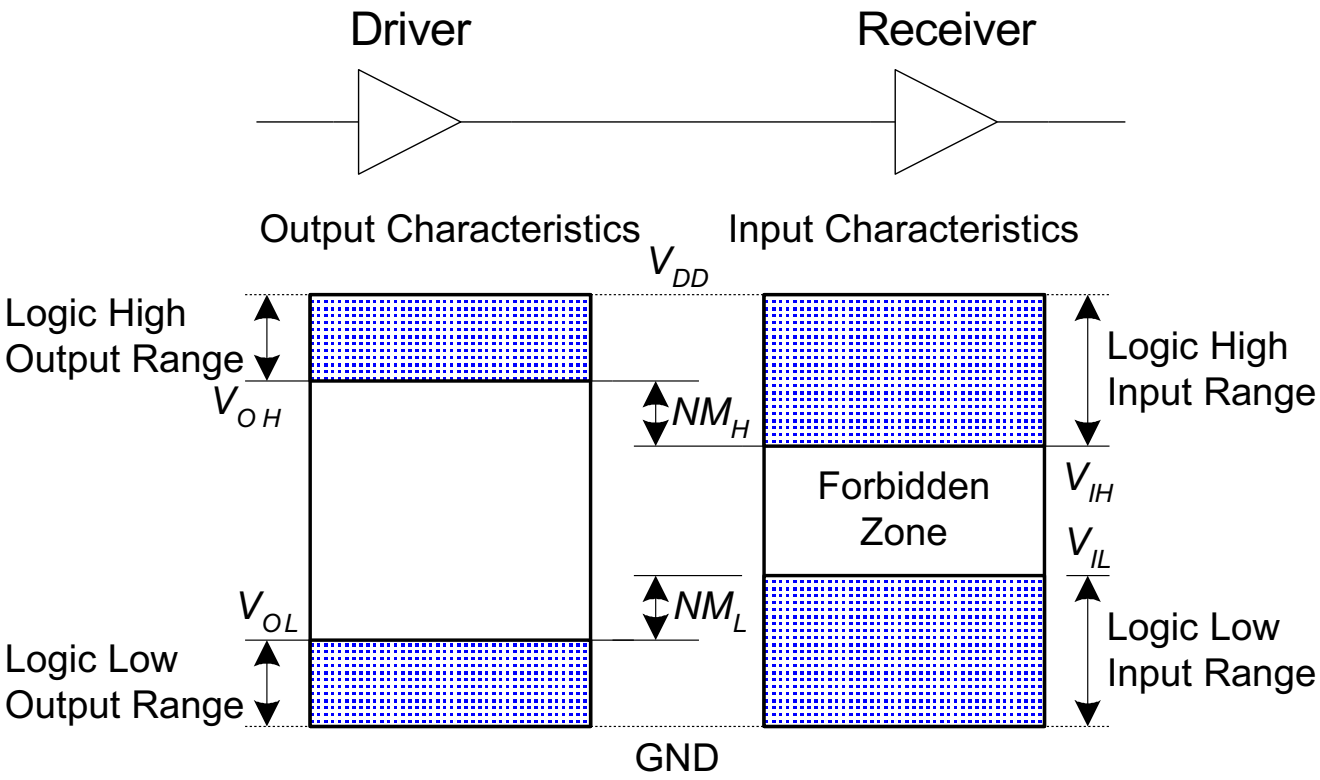
The Static Discipline

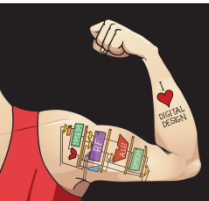
- With logically valid inputs, every circuit element must produce logically valid outputs

- Use limited ranges of voltages to represent discrete values

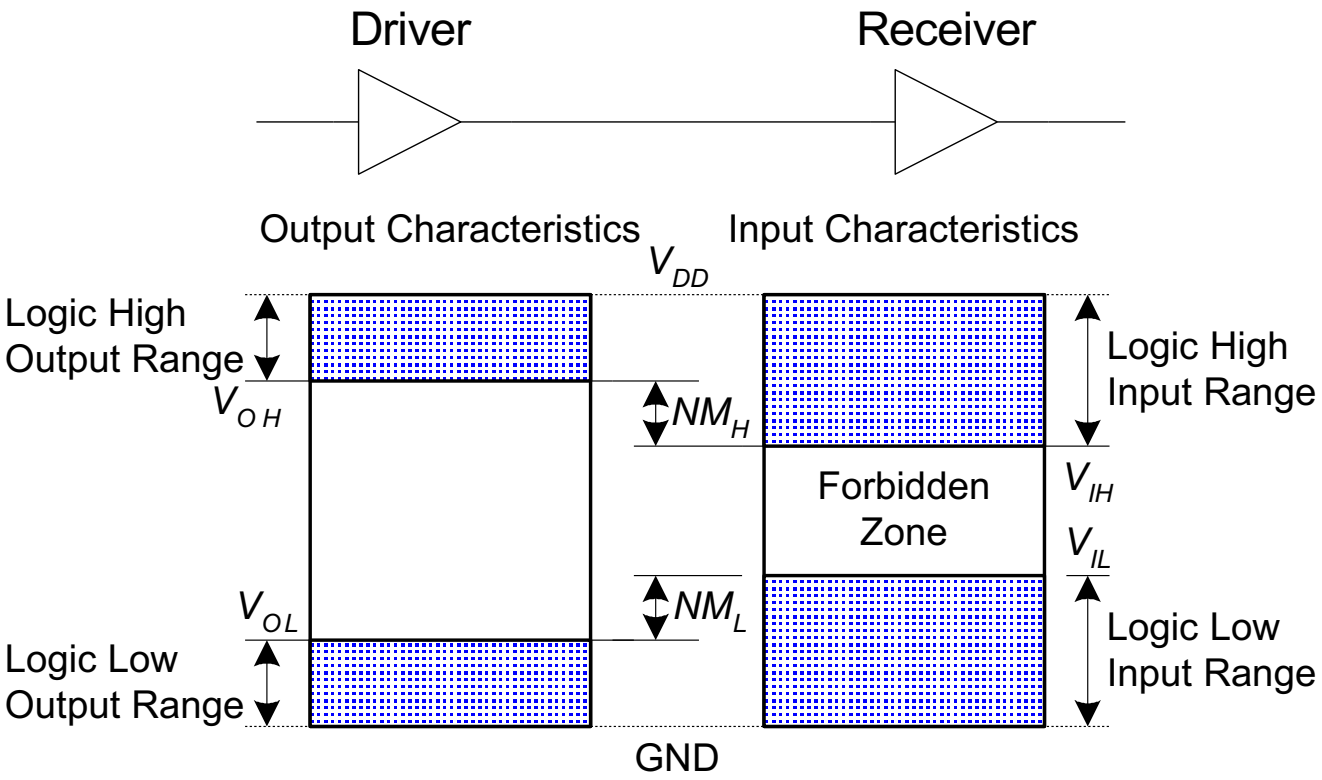


Noise Margins



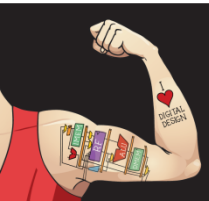


Noise Margins



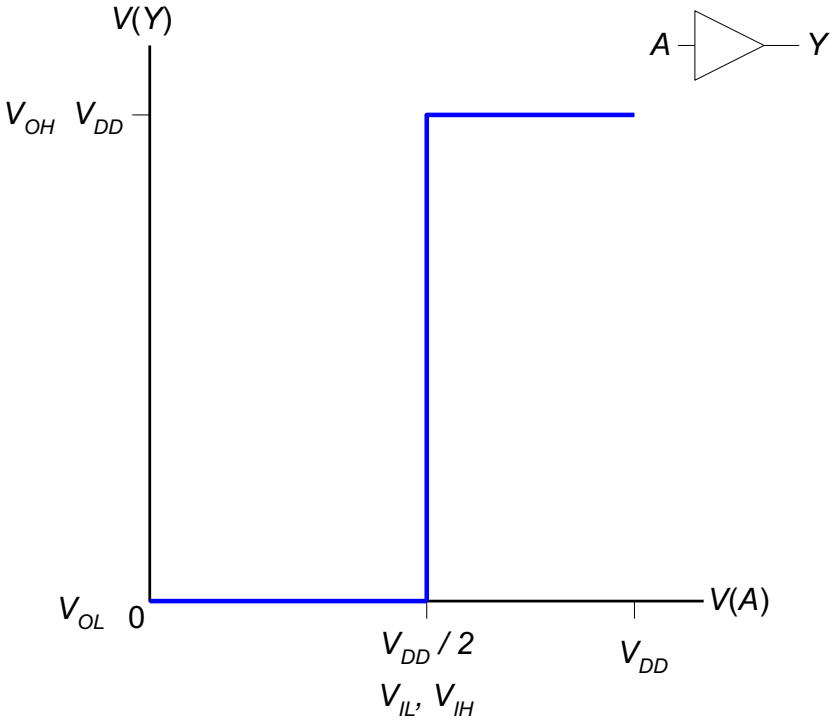
High Noise Margin: NM_H =

Low Noise Margin: NM_L =

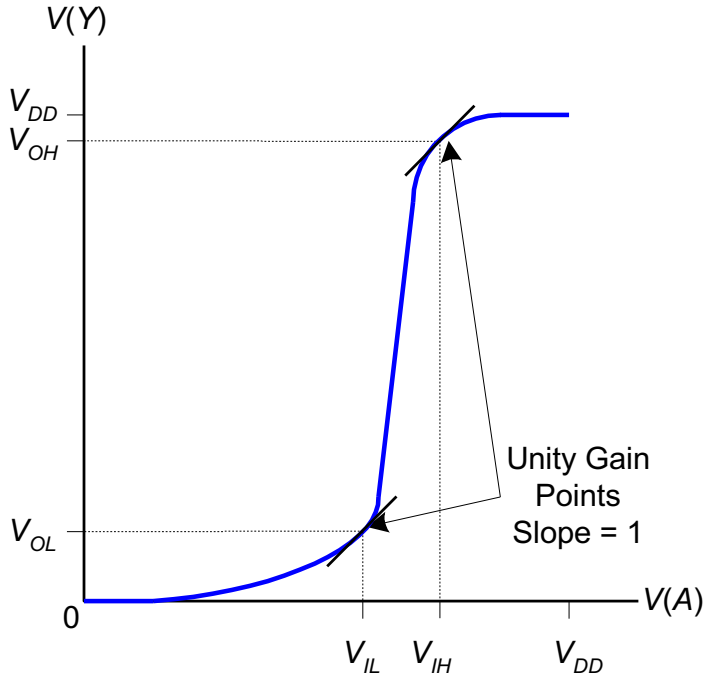


DC Transfer Characteristics

Ideal Buffer:

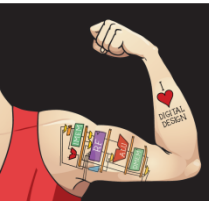


Real Buffer:

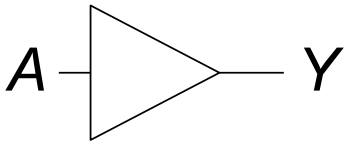


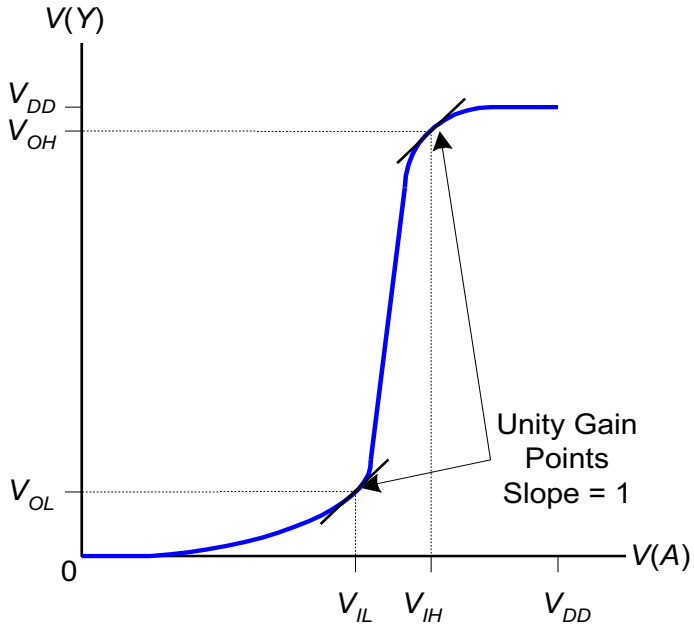
$$NM_H = NM_L = V_{DD}/2$$

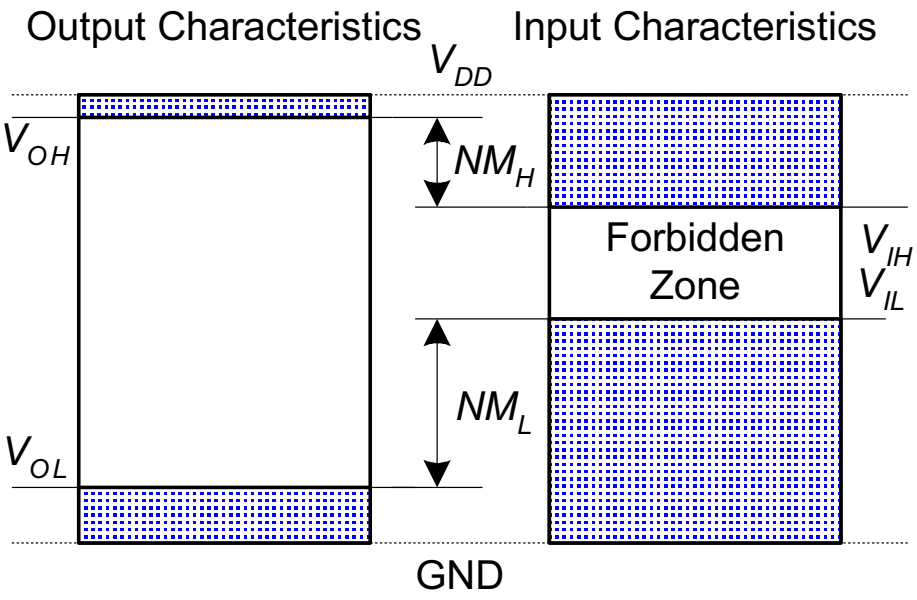
$$NM_H, NM_L < V_{DD}/2$$



DC Transfer Characteristics

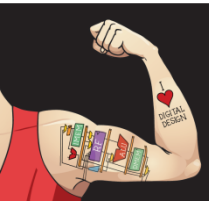






V_{DD} Scaling

- In 1970's and 1980's, V_{DD} = 5 V
- V_{DD} has dropped
  - Avoid frying tiny transistors
  - Save power
- 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, …
  - Be careful connecting chips with different supply voltages



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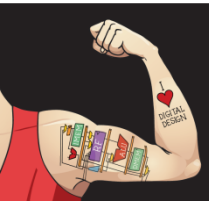
- 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, …
  - Be careful connecting chips with different supply voltages

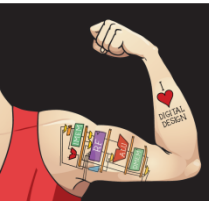
Chips operate because they contain magic smoke

Proof: if the magic smoke is let out, the chip stops working



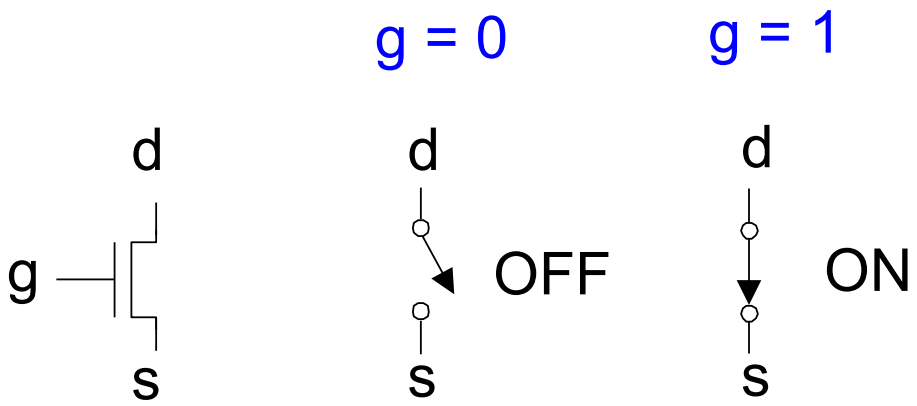
Logic Family Examples

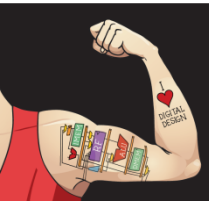
Logic Family	V_{DD}	V_{IL}	V_{IH}	V_{OL}	V_{OH}
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVCMOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7



Transistors

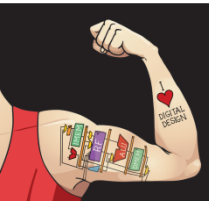
- Logic gates built from transistors
- 3-ported voltage-controlled switch
  - 2 ports connected depending on voltage of 3rd
  - d and s are connected (ON) when g is 1





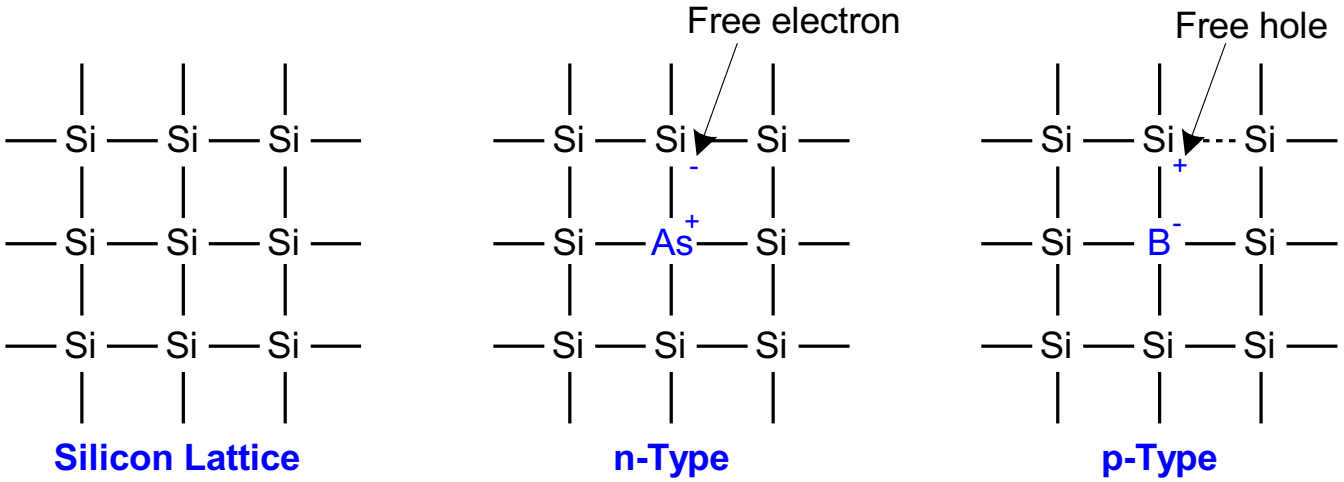
Robert Noyce, 1927-1990

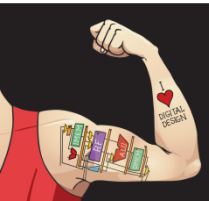
- Nicknamed “Mayor of Silicon Valley”
- Cofounded Fairchild Semiconductor in 1957
- Cofounded Intel in 1968
- Co-invented the integrated circuit



Silicon

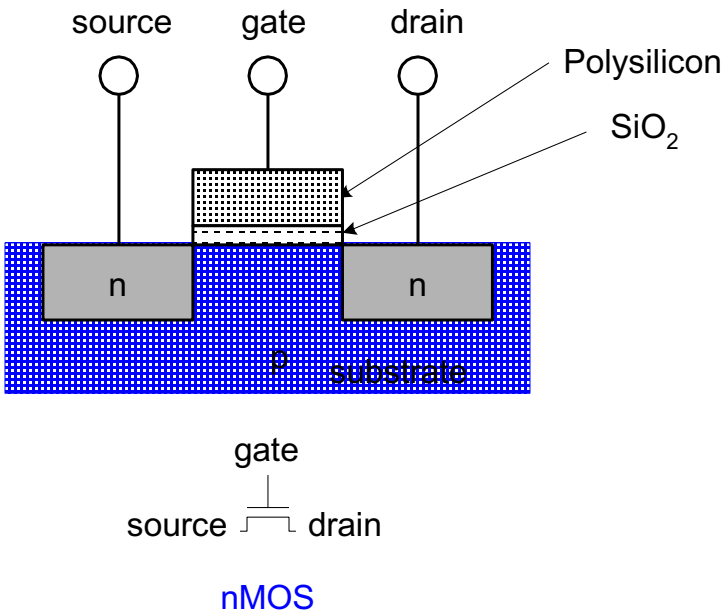
- Transistors built from silicon, a semiconductor
- Pure silicon is a poor conductor (no free charges)
- Doped silicon is a good conductor (free charges)
  - n-type (free ***n***egative charges, electrons)
  - p-type (free ***p***ositive charges, holes)

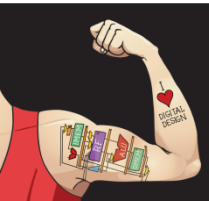




MOS Transistors

- **Metal oxide silicon (MOS) transistors:**
  - Polysilicon (used to be **metal**) gate
  - **Oxide** (silicon dioxide) insulator
  - Doped **silicon**

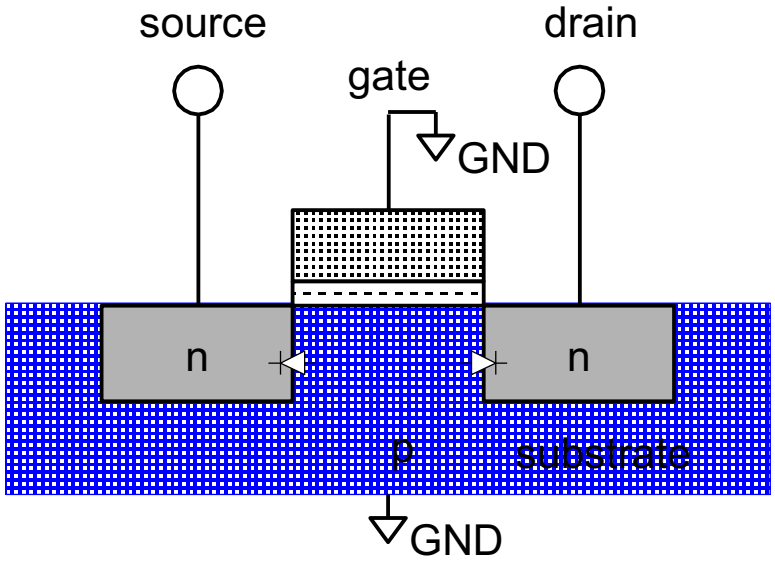




Transistors: nMOS

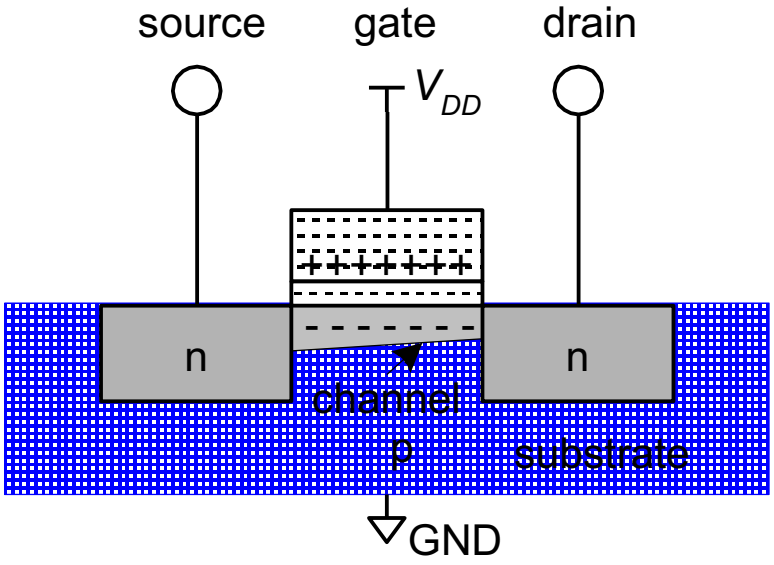
Gate = 0

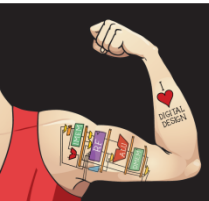
OFF (no connection between source and drain)



Gate = 1

ON (channel between source and drain)

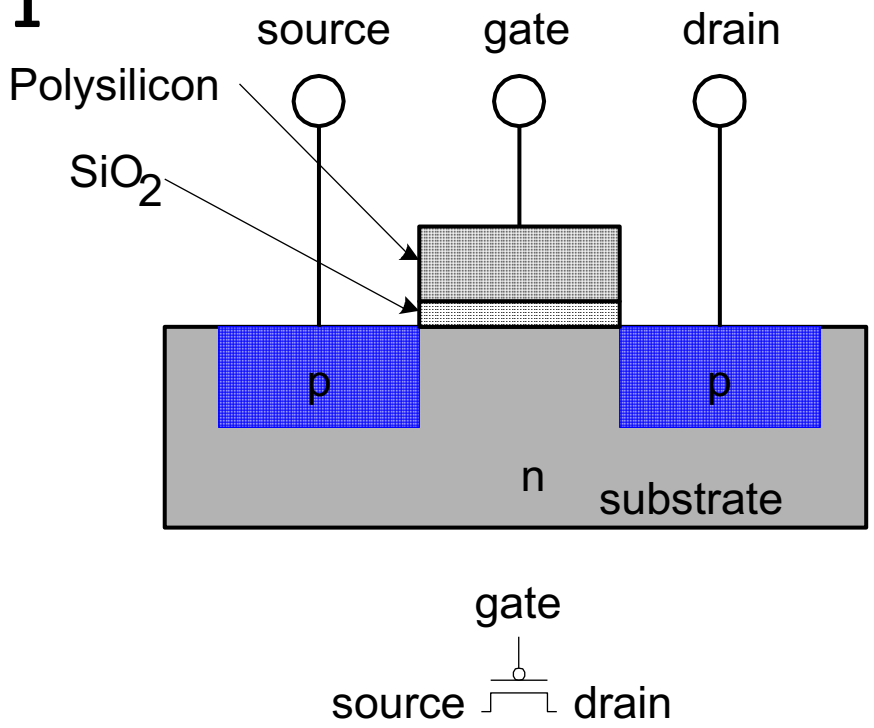


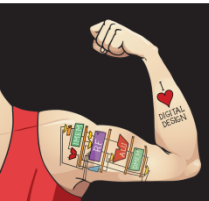


Transistors: pMOS

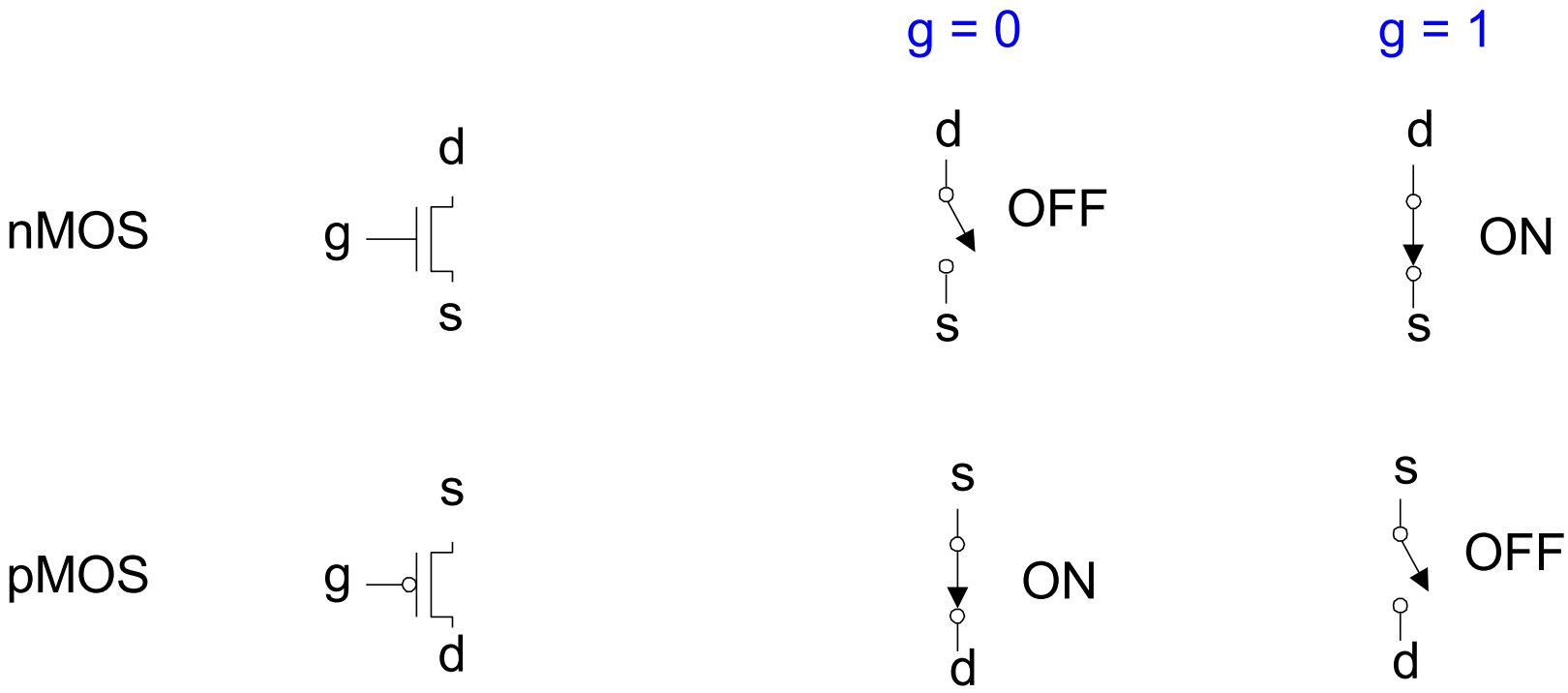
pMOS transistor is opposite

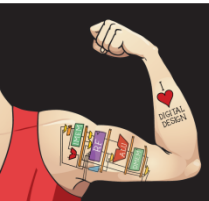
- **ON** when **Gate = 0**
- **OFF** when **Gate = 1**





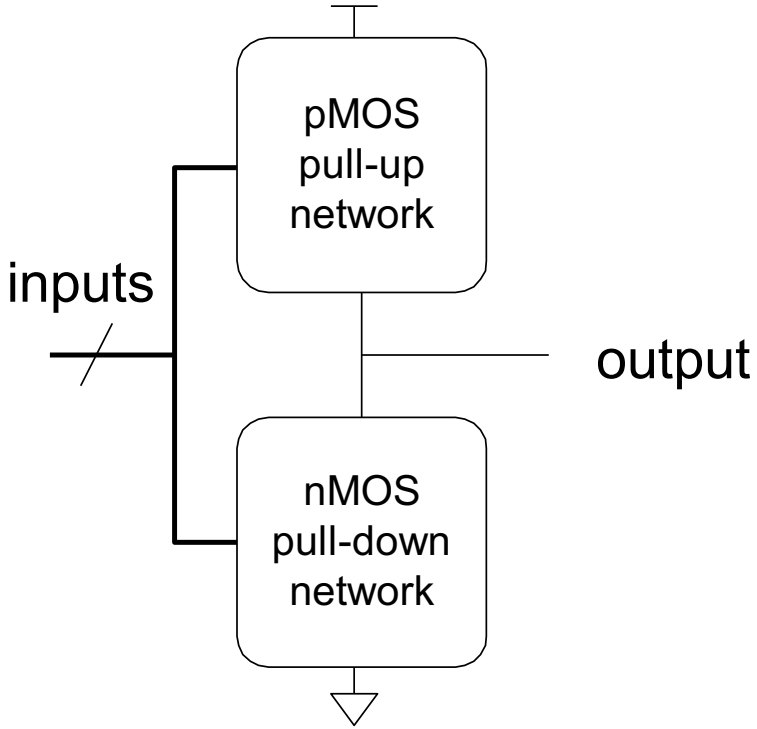
Transistor Function

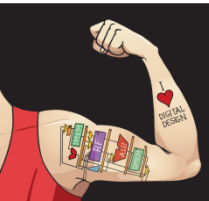




Transistor Function

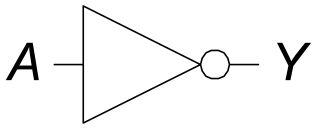
- **nMOS**: pass good **0**'s, so connect source to GND
- **pMOS**: pass good **1**'s, so connect source to V_{DD}





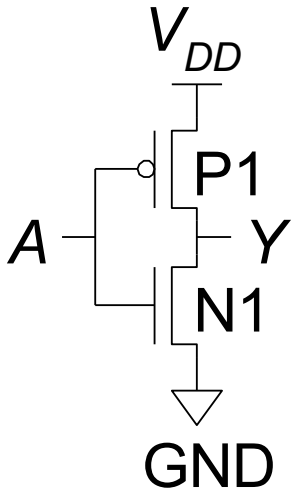
CMOS Gates: NOT Gate

NOT

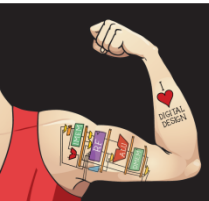


$Y = \overline{A}$

A	Y
0	1
1	0

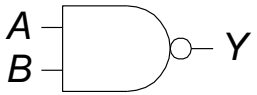


A	P1	N1	*Y*
0			
1			



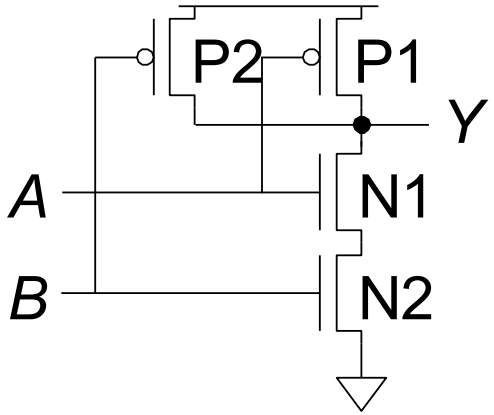
CMOS Gates: NAND Gate

NAND

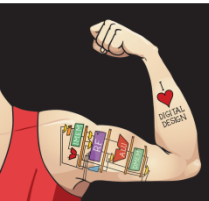


$Y = \overline{AB}$

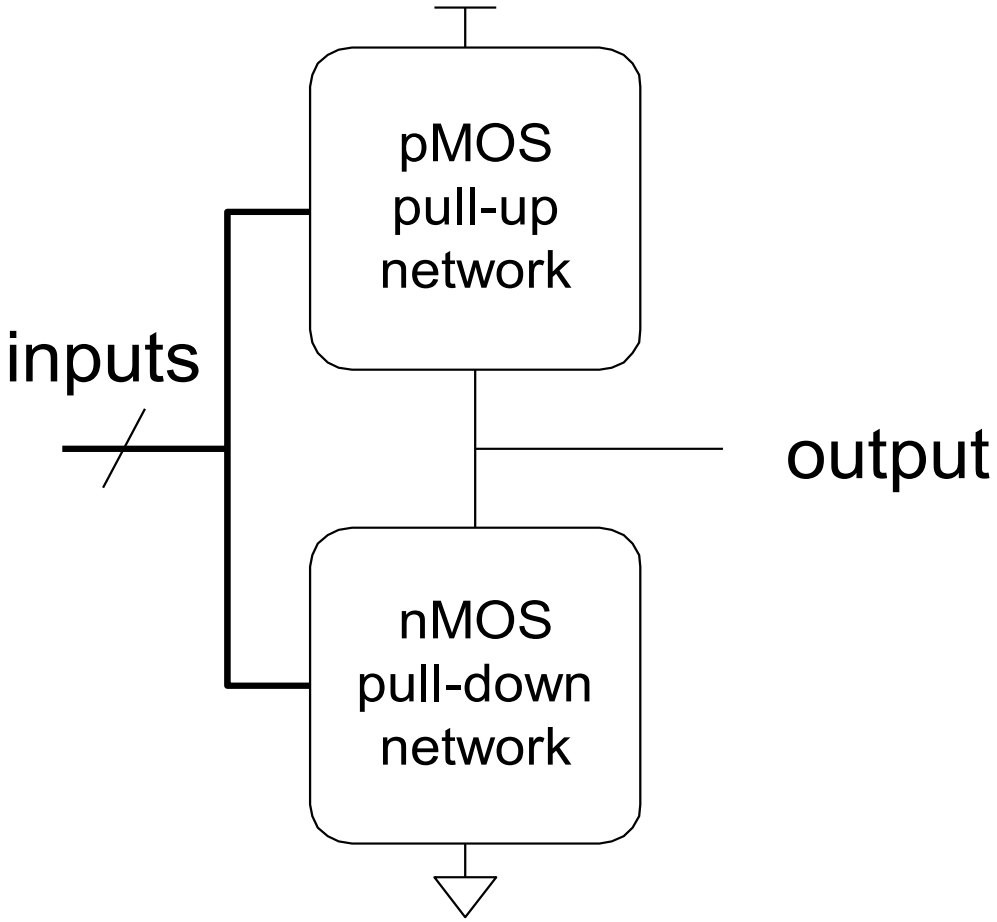
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

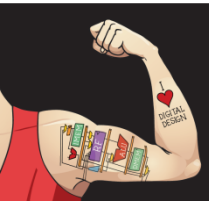


A	*B*	P1	P2	N1	N2	*Y*
0	0					
0	1					
1	0					
1	1					



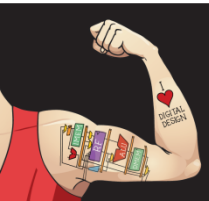
CMOS Gate Structure





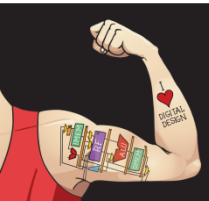
NOR3 Gate

How do you build a three-input NOR gate?



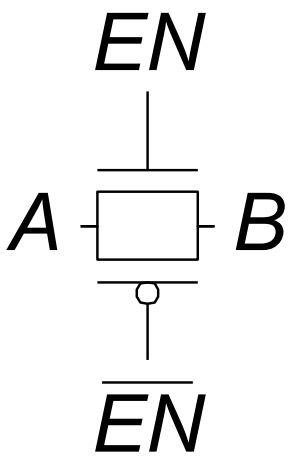
AND2 Gate

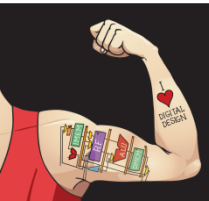
How do you build a two-input AND gate?



Transmission Gates

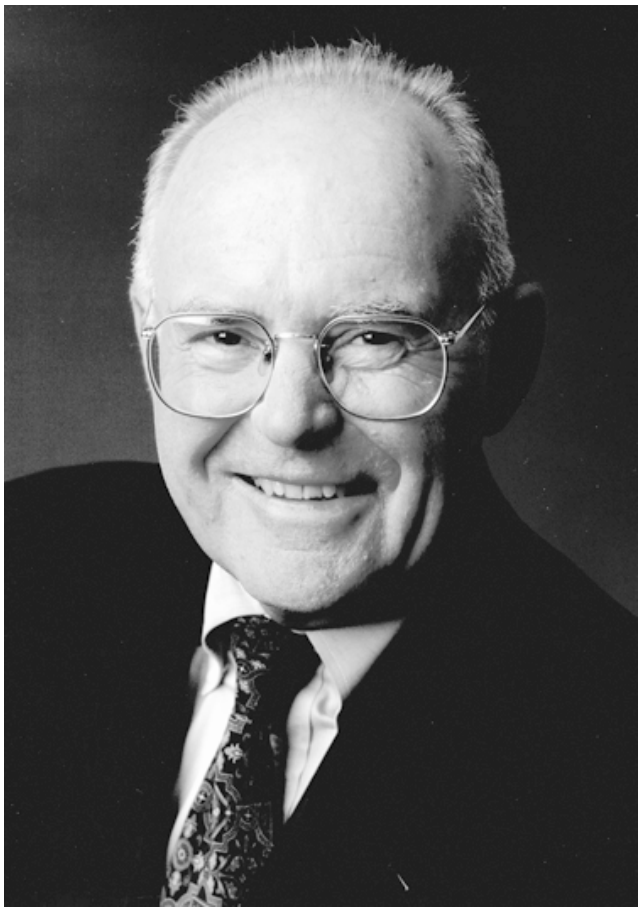
- nMOS pass 1's poorly
- pMOS pass 0's poorly
- Transmission gate is a better switch
  - passes both 0 and 1 well
- When *EN* = 1, the switch is ON:
  - *EN* = 0 and *A* is connected to *B*
- When *EN* = 0, the switch is OFF:
  - *A* is not connected to *B*

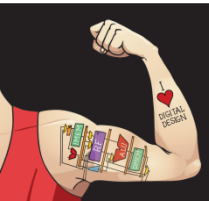




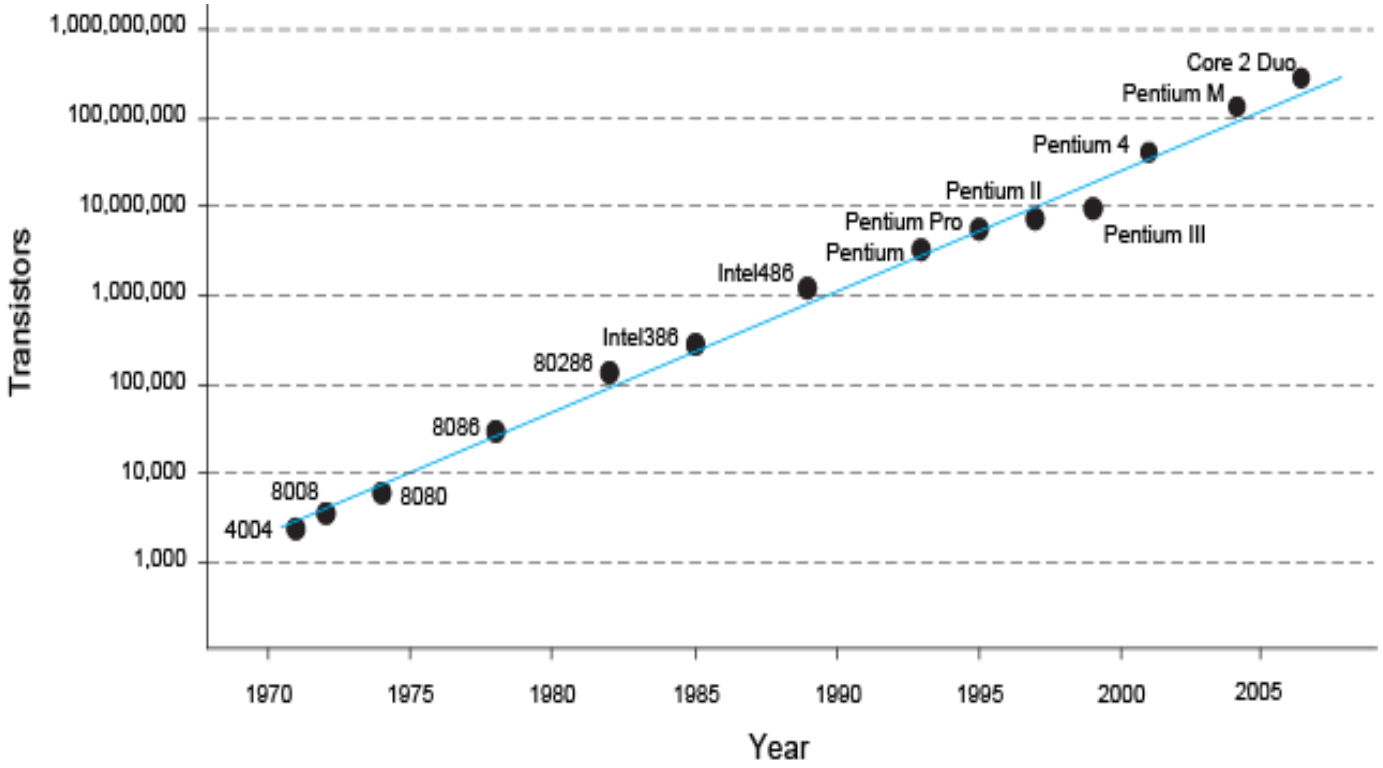
Gordon Moore, 1929-

- Cofounded Intel in 1968 with Robert Noyce.
- **Moore's Law:** number of transistors on a computer chip doubles every year (observed in 1965)
- Since 1975, transistor counts have doubled every two years.



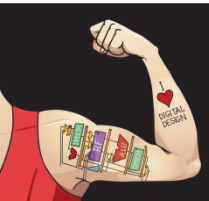


Moore's Law



"If the automobile had followed the same development cycle as the computer, a Rolls-Royce would today cost $100, get one million miles to the gallon, and explode once a year . . ." (Robert Cringely, Infoworld)

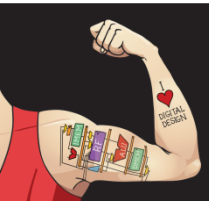
– Robert Cringley



Power Consumption

Power = Energy consumed per unit time

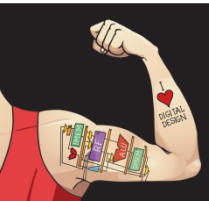
- Dynamic power consumption
- Static power consumption



Dynamic Power Consumption

- **Power to charge transistor gate capacitances**
  - Energy required to charge a capacitance, C, to V_{DD} is CV_{DD}^2
  - Circuit running at frequency f: transistors switch (from 1 to 0 or vice versa) at that frequency
  - Capacitor is charged $f/2$ times per second (discharging from 1 to 0 is free)
- **Dynamic power consumption:**

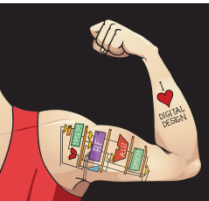
$$P_{dynamic} = \tfrac{1}{2}CV_{DD}^2 f$$



Static Power Consumption

- Power consumed when no gates are switching
- Caused by the *quiescent supply current*, I_{DD} (also called the *leakage current*)
- Static power consumption:

$$P_{static} = I_{DD} V_{DD}$$



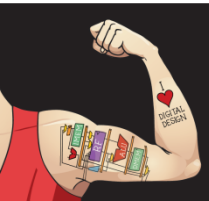
Power Consumption Example

- Estimate the power consumption of a mobile phone running Angry Birds
  - V_{DD} = 0.8 V
  - C = 5 nF
  - f = 2 GHz
  - I_{DD} = 10 mA

$$P = \tfrac{1}{2}CV_{DD}^2 f + I_{DD}V_{DD}$$

$$= \tfrac{1}{2}(5\text{ nF})(0.8\text{ V})^2(2\text{ GHz}) + (10\text{ mA})(0.8\text{ V})$$

$$= (3.2 + 0.008)\text{ W} \approx 3.2\text{ W}$$



Datasheets

- **Datasheets are a contract between the manufactuer and the user.**

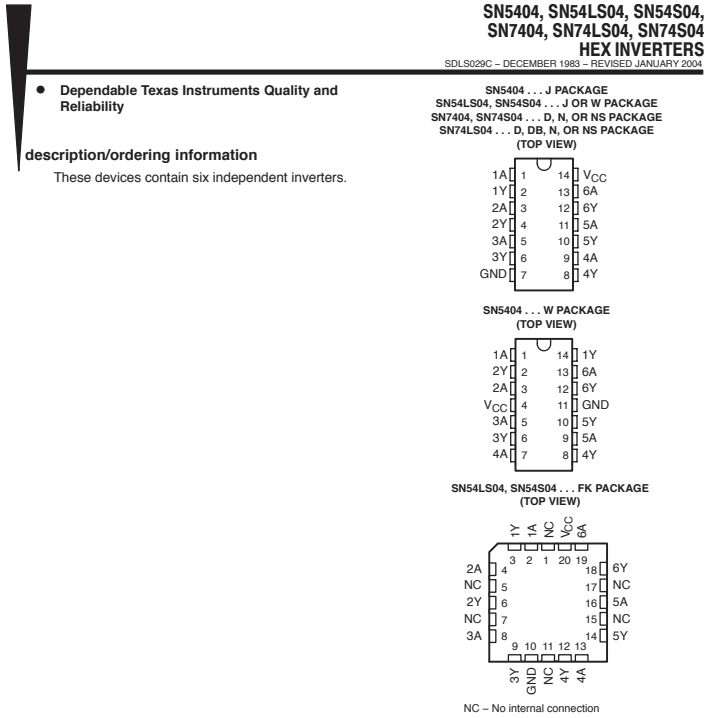
- **74LS04 has six NOT gates**
- **Pinout**
  - **Input A, output Y**
  - **Also hook up VCC and GND**

74-series are logic gates

LS: Low power Shottky

HC: High speed CMOS

04: six NOT gates



SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS

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- Dependable Texas Instruments Quality and Reliability

description/ordering information

These devices contain six independent inverters.

SN5404 . . . J PACKAGE
SN54LS04, SN54S04 . . . J OR W PACKAGE
SN7404, SN74S04 . . . D, N, OR NS PACKAGE
SN74LS04 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)

1A	1	14	V_{CC}
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

SN5404 . . . W PACKAGE
(TOP VIEW)

1A	1	14	1Y
2Y	2	13	6A
2A	3	12	6Y
V_{CC}	4	11	GND
3A	5	10	5Y
3Y	6	9	5A
4A	7	8	4Y

SN54LS04, SN54S04 . . . FK PACKAGE
(TOP VIEW)

			1Y	1A	NC	V_{CC}	6A		
			3	2	1	20	19		
2A	4							18	6Y
NC	5							17	NC
2Y	6							16	5A
NC	7							15	NC
3A	8							14	5Y
		9	10	11	12	13			
		3Y	GND	NC	4Y	4A			

NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
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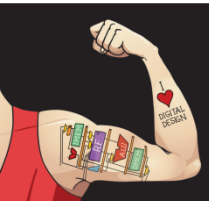
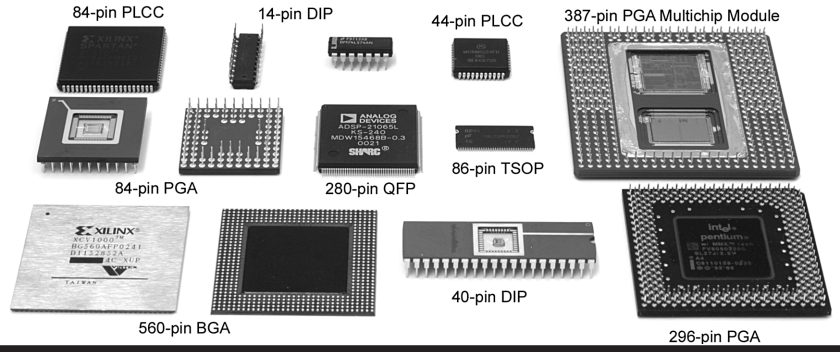
1



Datasheets

- Chips are available in plastic or ceramic packages with different temperature ratings.
- Dual Inline Package (DIP)
- Small Outline IC (SOIC)
- Small Outline Package (SOP)
- Leadless Chip Carrier (LCC)



SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS

SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7404N	SN7404N
		Tube	SN74LS04N	SN74LS04N
		Tube	SN74S04N	SN74S04N
	SOIC – D	Tube	SN7404D	7404
		Tape and reel	SN7404DR	
		Tube	SN74LS04D	LS04
		Tape and reel	SN74LS04DR	
		Tube	SN74S04D	S04
		Tape and reel	SN74S04DR	
	SOP – NS	Tape and reel	SN7404NSR	SN7404
		Tape and reel	SN74LS04NSR	74LS04
		Tape and reel	SN74S04NSR	74S04
	SSOP – DB	Tape and reel	SN74LS04DBR	LS04
–55°C to 125°C	CDIP – J	Tube	SN5404J	SN5404J
		Tube	SNJ5404J	SNJ5404J
		Tube	SN54LS04J	SN54LS04J
		Tube	SN54S04J	SN54S04J
		Tube	SNJ54LS04J	SNJ54LS04J
		Tube	SNJ54S04J	SNJ54S04J
	CFP – W	Tube	SNJ5404W	SNJ5404W
		Tube	SNJ54LS04W	SNJ54LS04W
		Tube	SNJ54S04W	SNJ54S04W
	LCCC – FK	Tube	SNJ54LS04FK	SNJ54LS04FK
		Tube	SNJ54S04FK	SNJ54S04FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

TEXAS INSTRUMENTS
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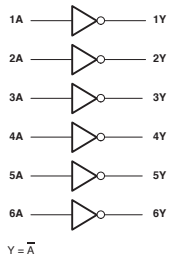
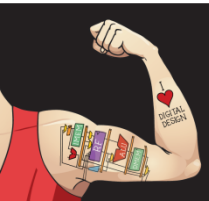
ELSEVIER

Datasheets

- **Six NOT gates**
- **Input A, output Y**

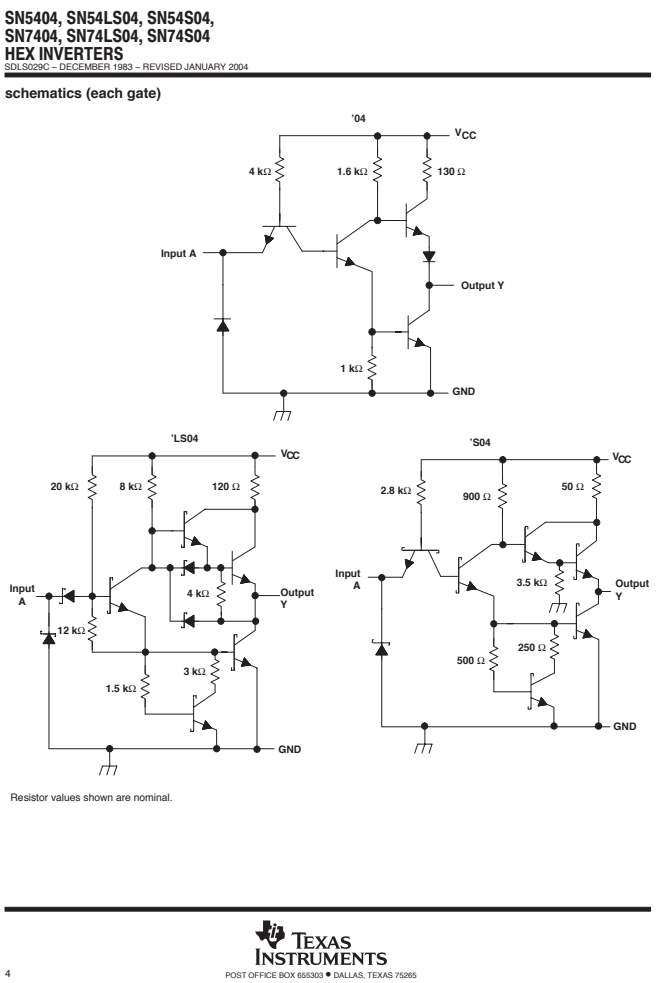
logic diagram (positive logic)





Datasheets

- **Internal structure**
  - **Not too important for you.**
  - **NPN transistor at middle and resistors above and below comprise the inverter**
  - **NPN transistors on right form an output stage for driving more current**



SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS
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schematics (each gate)

Resistor values shown are nominal.

TEXAS INSTRUMENTS
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Datasheets

- **Absolute Maximums specify when the chip will catch on fire or suffer permanent damage. It is not guaranteed to function correctly near these levels. Don't use for design purposes.**
- **Recommended Operating Conditions say how it should be used.**
- **Different vendors have different names for conditions**
  - **Use some common sense to interpret**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: '04, 'S04 . . . . . 5.5 V
'LS04 . . . . . 7 V
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN5404			SN7404			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–0.4			–0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡			SN5404			SN7404			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	V_{CC} = MIN,	I_I = –12 mA				–1.5			–1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = 0.8 V,	I_{OH} = –0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.4 V				40			40	µA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				–1.6			–1.6	mA
I_{OS}¶	V_{CC} = MAX			–20		–55	–18		–55	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			6	12		6	12	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			18	33		18	33	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

Datasheets

- **Note 74LS vs. 74**
- **Supply voltage (V_{CC})**
- **Logic levels (V_{IH}, V_{IL}, V_{OH}, V_{OL})**
- **Currents**
  - **Output (I_{OH}, I_{OL}, I_{OS})**
  - **Input (I_I, I_H, I_L)**
  - **Supply (I_{CCH}, I_{CCL})**
- **Propagation Delay (t_{PLH}, t_{PHL})**

SN5404, SN54LS04, SN54S04,
SN7404, SN74LS04, SN74S04
HEX INVERTERS
SDLS029C – DECEMBER 1983 – REVISED JANUARY 2004

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN5404 SN7404 MIN	SN5404 SN7404 TYP	SN5404 SN7404 MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	

recommended operating conditions (see Note 3)

		SN54LS04 MIN	SN54LS04 NOM	SN54LS04 MAX	SN74LS04 MIN	SN74LS04 NOM	SN74LS04 MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS04 MIN	SN54LS04 TYP‡	SN54LS04 MAX	SN74LS04 MIN	SN74LS04 TYP‡	SN74LS04 MAX	UNIT
V_{IK}	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	V_{CC} = MIN,	V_{IL} = MAX,	I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN,	V_{IH} = 2 V	I_{OL} = 4 mA		0.25	0.4			0.4	V
			I_{OL} = 8 mA					0.25	0.5	
I_I	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX,	V_I = 0 V			1.2	2.4		1.2	2.4	mA
I_{CCL}	V_{CC} = MAX,	V_I = 4.5 V			3.6	6.6		3.6	6.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS04 SN74LS04 MIN	SN54LS04 SN74LS04 TYP	SN54LS04 SN74LS04 MAX	UNIT
t_{PLH}	A	Y	R_L = 2 kΩ, C_L = 15 pF		9	15	ns
t_{PHL}					10	15	

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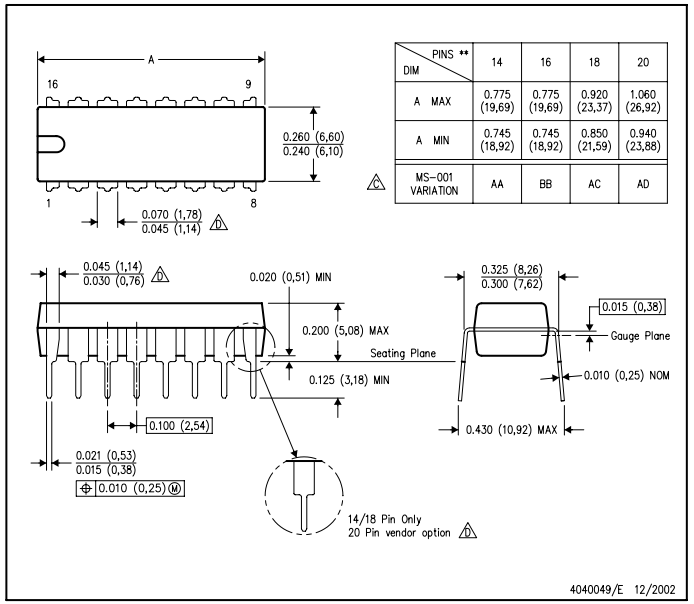
Datasheets

- **Mechanical data important when you are designing a printed circuit board.**
- **Make sure the pins fit your board!**

MECHANICAL DATA

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
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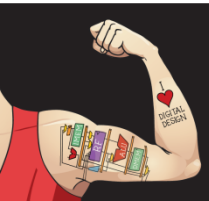
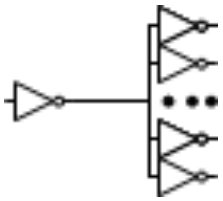


Example: Fanout

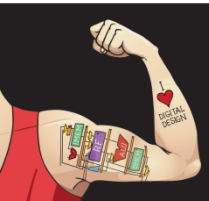
What is the maximum fanout for a 74LS04 NOT gate?



Solution:

Maximum current into a 74LS04 is I_{IL} = 0.4 mA.
Output voltage V_{OL} is guaranteed at I_{OL} = 8 mA

Hence, maximum fanout is I_{OL} / I_{IL} = 20.



Example: Power Consumption

One 74LS04 NOT gate drives 20 identical gates. V_{CC} = 5V. What is the power consumption of the entire system if the input to the first gate switches at 1 MHz?

Static Power:

Each gate draws $I_{CC} = (I_{CCL} + I_{CCH})/2 = (6.6 + 2.4\ mA)/2 = 4.5\ mA$

I_{static} = (21 gates)(4.5 mA/gate) = 94.5 mA

P_{static} = 94.5 mA * 5 V = 472.5 mW

Dynamic Power

C_{in} is not specified. Assume 15 pF/gate * 20 gates = 300 pF.

$P = CV_{DD}2f$ = (300x10-12)(52)(1x106) = 7.5 mW

$P_{total} = P_{static} + P_{dynamic}$ = 480 mW

TTL power is primarily static