

Digital Electronics & Computer Engineering (E85)

Harris

Spring 2018

Midterm

CALVIN AND HOBBS • Bill Watterson



This is a closed-book take-home exam. Electronic devices including calculators are not allowed. You are permitted one 8.5x11" sheet of paper with notes.

You are bound by the HMC Honor Code while taking this exam.

The exam is intended to be doable in 75 minutes, but everyone in the class is granted extra time up to 120 contiguous minutes so you should not feel time pressure if you have prepared adequately.

Return the exam under Prof. Harris' door no later than Wednesday 2/28 at 11 am.

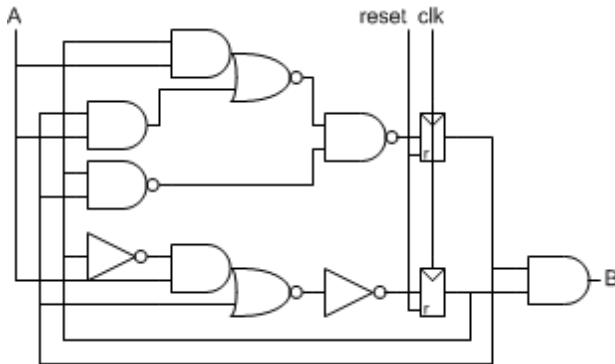
Along side each question, the number of points is written in brackets. The entire exam is worth 20 points. Plan your time accordingly. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. Show your work for partial credit.

Name: _____

Score

Page 2: _____ / 3
Page 3: _____ / 7
Page 4: _____ / 4
Page 5: _____ / 6
Total: _____ / 20

Consider the following circuit:



The system operates on a 2 V power supply. Each element (gate or flop) draws 10 nA of quiescent supply current. Each input pin of each element has 5 fF of capacitance, and the other capacitances are negligible. Conservatively assume that every wire toggles once per cycle, except reset, which is 0 during normal operation.

The delays of each gate are given below. The flip-flop has a setup time of 22 ps, a hold time of 3 ps, and clock-to-Q propagation and contamination delays of 13 and 8 ps.

Element	Propagation Delay (ps)	Contamination Delay (ps)
NOT	10	5
NAND2 / NOR2	15	9
NAND3 / NOR3	20	12
AND2 / OR2	24	14
AND3 / OR3	28	16
AOI	30	11

[1] Is this circuit combinational or sequential? **Combinational** **Sequential**

[2] The circuit includes two AND-OR-INVERT (AOI) gates performing $Y = \sim(AB + C)$. Sketch a transistor-level implementation of an AOI using as few transistors as possible.

Circuit Diagram

[2] What is the minimum clock period for which the circuit will work in the absence of clock skew?

_____ ps

[2] How much clock skew could the system experience before it might violate a hold time?

_____ ps

[3] Redesign the circuit to run as fast as possible. You may use any gates in the table above. Sketch your new circuit. What clock period can you achieve in the absence of skew?

(new circuit)

_____ ps

[1] How many logic elements (LEs) are required to implement this circuit on a Cyclone FPGA?

_____ **LEs**

[3] At what frequency is dynamic and static power equal? (If you are unsure of any assumptions you need to make, state your assumptions.)

_____ **Hz**

[3] Sketch a state transition diagram for the circuit.

State Transition Diagram

[3] Write behavioral Verilog for the circuit based on the state transition diagram you sketched.

```
module midterm(input  logic clk, reset, a,  
               output logic b);
```

```
endmodule
```