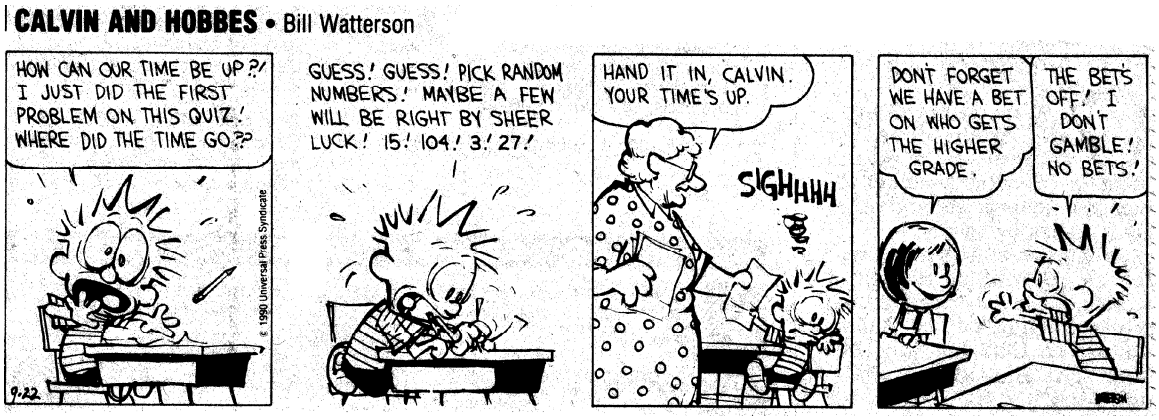
Digital Electronics & Computer Engineering (E85)

Harris Spring 2007

Midterm



This is a closed-book exam. You are permitted a calculator and one 8.5x11" page of paper with notes.

Along side each question, the number of points is written in brackets. The entire exam is worth 30 points. Plan your time accordingly. All work and answers should be written directly on this examination booklet. Use the backs of pages if necessary. Write neatly; illegible answers will be marked wrong. Show your work for partial credit.

Name: _____

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Page 2-3: _____ /10

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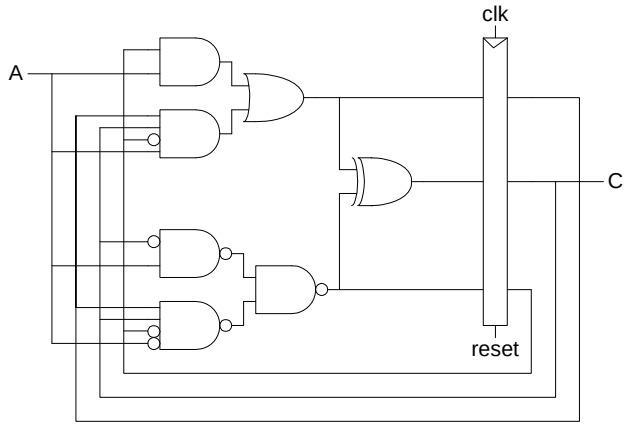
Total: _____ /30

The proctors have noticed a distressing number of cranky freshmen at Harvey Mudd College. They observe that the crankiness seems to be associated with sleep deprivation. No less a proctor than the renown Andrew Danowitz designs a finite state machine to help predict whether the Mudder will be cranky. The FSM has a single input, A, that is TRUE if the freshman has pulled an all-nighter. It has a single output, C, that is TRUE when it predicts that the freshman will be cranky. Unfortunately, Andrew himself pulled an all-nighter before building the circuit, and it is unnecessarily complex, as shown below.



1. [3] Draw a state transition diagram for the FSM.

2. [2] Write a state transition table for the FSM. Replace the state encoding with a new encoding of your choice that uses the minimum number of bits of state.

3. [3] Sketch a simpler FSM performing the same function. It should use the minimum possible number of flip-flops and should use minimal sum-of-products logic.

4. [2] The lab ran out of logic gates. Show how to implement the next state logic using only 4-input multiplexers.

When two floating point numbers are subtracted, the mantissa may experience massive cancellation. If so, it may have to be left-shifted by many columns to produce a normalized result with a leading 1.

5. [2] Ben Bitdiddle observes that when computing X – Y, the result must be left-shifted by 3 positions to be normalized. X is a single-precision floating point number with the hexadecimal representation 3F800000. Give an example of a number Y for which Ben's observation is correct. Express your answer in hexadecimal.

Y _____

A Leading One Detector circuit examines the result and produces an output indicating how much to shift to properly normalize the number. It also produces a Zero signal indicating that the two numbers were equal and completely canceled when subtracted, producing a zero answer. Alyssa P. Hacker is building a low-precision floating point engine with only 8 bits of mantissa. She writes the following Verilog code for her Leading One Detector

```
module lod(input      [7:0] mantissa,
           output reg [2:0] shiftamt,
           output           zero);

  assign zero = (mantissa == 8'b0);
  always @(mantissa)
    casez (mantissa)
      8'b1???????: shiftamt = 3'b000;
      8'b01??????: shiftamt = 3'b001;
      8'b001?????: shiftamt = 3'b010;
      8'b0001????: shiftamt = 3'b011;
      8'b00001???: shiftamt = 3'b100;
      8'b000001??: shiftamt = 3'b101;
      8'b0000001?: shiftamt = 3'b110;
      default:     shiftamt = 3'b111;
    endcase
endmodule
```

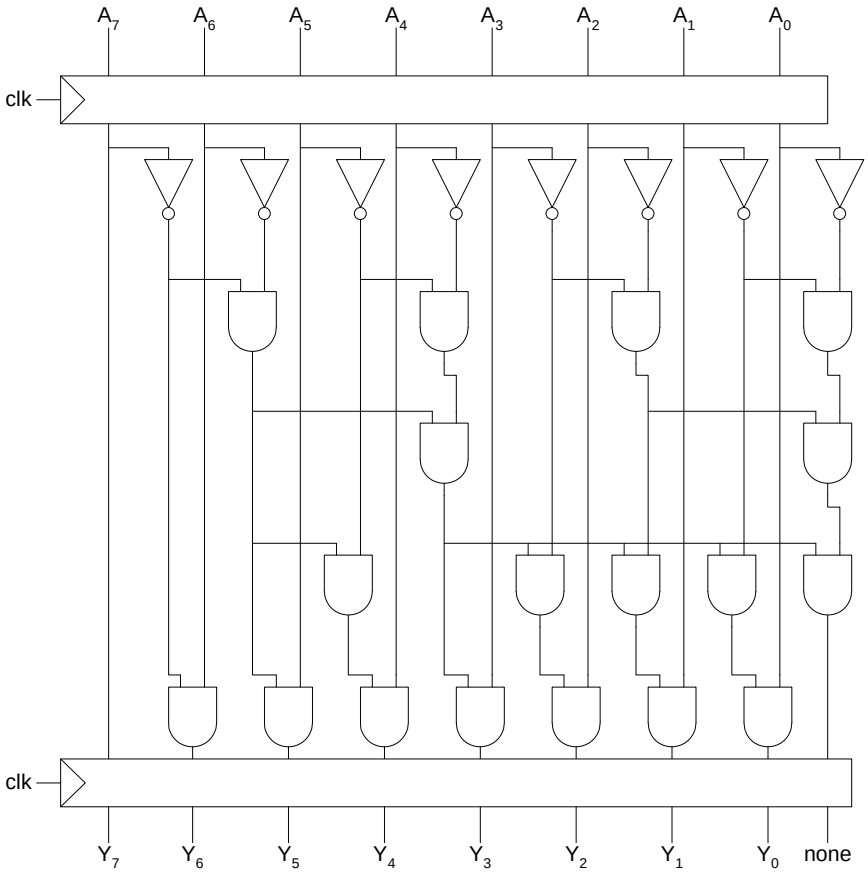
6. [3] Write minimal sum-of-products form Boolean equation for shamt[0]. Use abbreviations such as m_7 to indicate mantissa[7] for convenience.

shamt[0] = _____

Ben suggests using a priority circuit in place of the Leading One Detector. A priority circuit takes an N-bit input, A, and produces an N-bit output, Y, and a single-bit output, NONE. Exactly one of the output bits is TRUE, corresponding to the most significant input that is TRUE. If none of the inputs are TRUE, the NONE output is TRUE instead, and Y is all 0's. The most significant bit has the highest priority. For example, if A = 01011001, then Y = 01000000.

Ben wants to build a priority circuit using gates with no more than 2 inputs, and he would like the delay to increase only with the logarithm of the number of bits. He proposes the following design. Alice points out that he has a mistake.

7. [3] Mark up Ben's design to fix the mistake.



The elements in the circuit have the following delays

Inverter: t_{pd} = 30 ps

t_{cd} = 20 ps

AND2: t_{pd} = 50 ps

t_{cd} = 35 ps

Flop: t_{pcq} = 40 ps

t_{ccq} = 15 ps

t_{setup} = 60 ps

t_{hold} = 25 ps

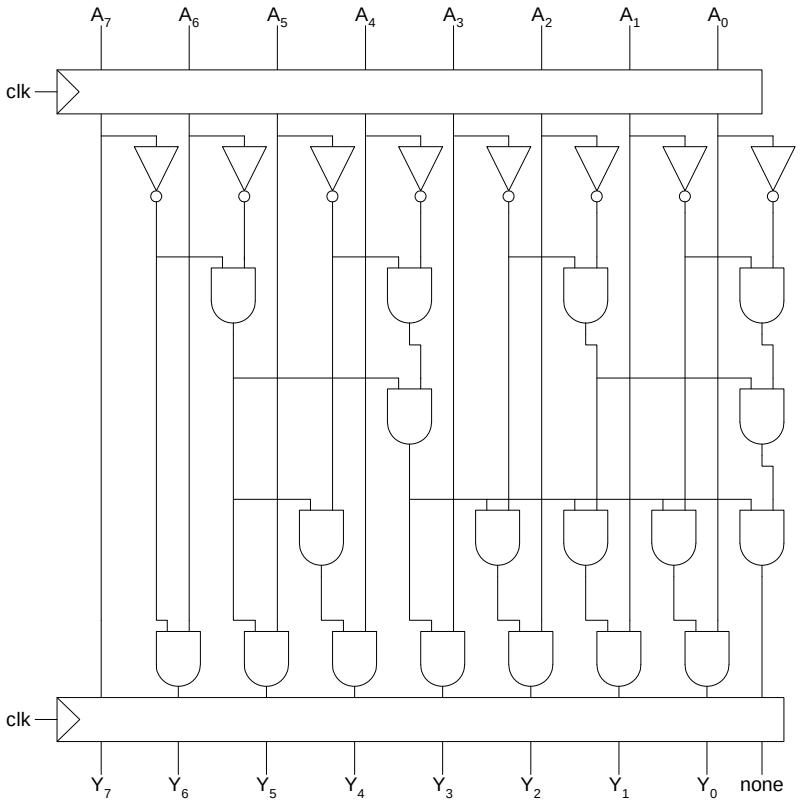
8. [3] Alice wants to know how fast the priority circuit can operate. Ben's error has no impact on the operating speed, so the answer shouldn't depend on whether you fixed the mistake or not. Find the minimum cycle time of the clock for which the circuit is guaranteed to operate correctly.

T_c _____

9. [2] Alice points out that Ben's circuit also has a hold time violation. By how much time is the hold time violated?

Time _____

10. [2] Mark up the priority circuit again to correct the hold time violation using as few modifications as necessary. If you wish to add more circuit elements, use only inverters, 2-input AND gates, and/or flip-flops.



A Caltech student accidentally walked in this exam and received a score of -9.8125 (punishment for not honoring the gods of partial credit). Write this number as a:

11. [2] 11 bit sign/magnitude number with 7 integer bits and 4 fraction bits

Sign/Magnitude Number _____

12. [3] 10-bit 2's complement number with 5 integer bits and 5 fraction bits

2's Complement Number _____