# Introduction to Computer Engineering (E85)
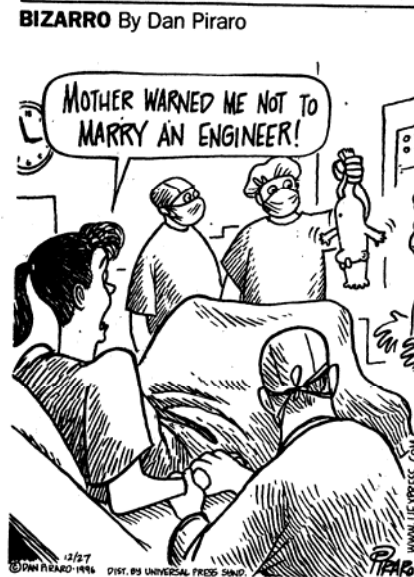
Harris                                                                 Fall 2007

**Problem Set 8**                          **Due: Wednesday, November 14**



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## 1) Textbook Problems

Do problems 7.2, 7.3(b,e), 7.6, 3.23 (FSM review).

For 7.2, consider the R-type instructions (`add`, `sub`, `and`, `or`, `slt`), `lw`, `sw`, `beq`, `j`, `addi`.

For 7.3(b): in `lui`, the machine code always specifies $0 for the rs (unused) source register.

Two copies of Figure 7.11 and Table 7.8 are attached for convenience on Exercise 7.3.

## 2) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for next semester's class.
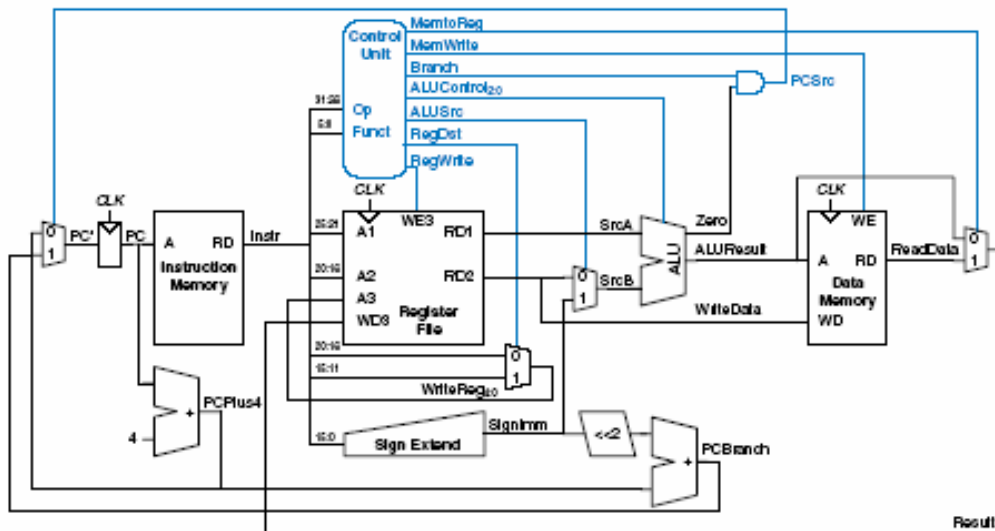
Figure 7.11 Complete single-cycle MIPS processor

Table 7.8 Main decoder truth table to mark up with changes

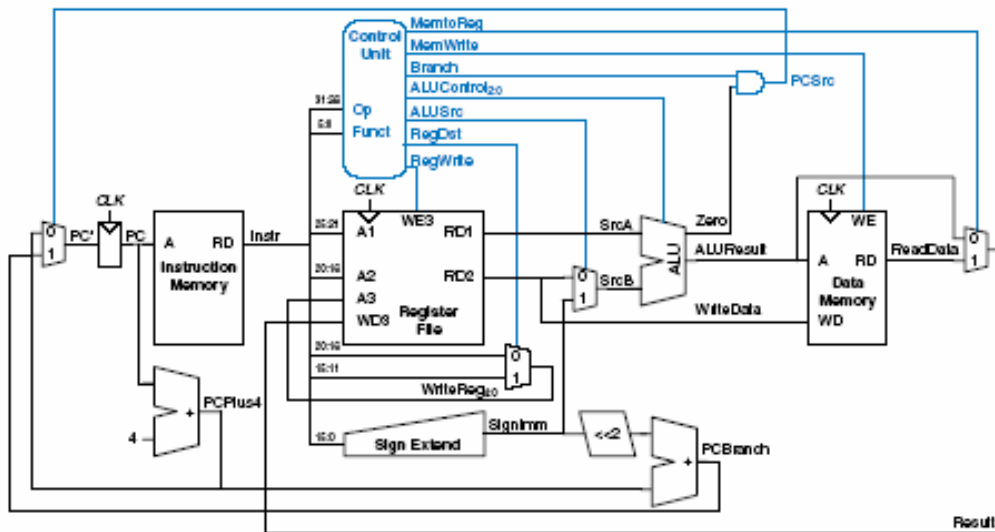| Instruction | Opcode | RegWrite | RegDst | ALUSrc | Branch | MemWrite | MemtoReg | ALUOp |
|---|---|---|---|---|---|---|---|---|
| R-type | 000000 | 1 | 1 | 0 | 0 | 0 | 0 | 10 |
| lw | 100011 | 1 | 0 | 1 | 0 | 0 | 1 | 00 |
| sw | 101011 | 0 | X | 1 | 0 | 1 | X | 00 |
| beq | 000100 | 0 | X | 0 | 1 | 0 | X | 01 |



Figure 7.11 Complete single-cycle MIPS processor

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| sw | 101011 | 0 | X | 1 | 0 | 1 | X | 00 |
| beq | 000100 | 0 | X | 0 | 1 | 0 | X | 01 |