Introduction to Computer Engineering (E85)
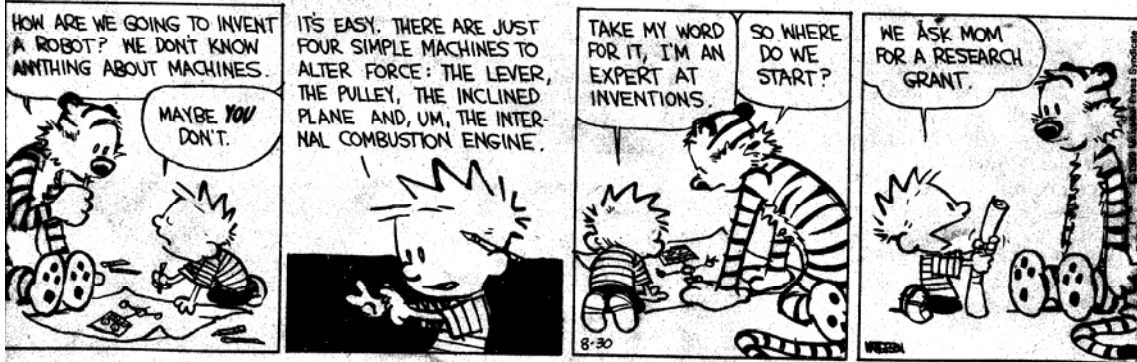
Harris   Fall 2007

Problem Set 6   **Due: Wednesday, October 31**

1) Textbook Problems

Do problems 5.27(a), 5.26(a) 5.29(b), 5.44(a-b), 5.48, 5.50(a,b,d,i),

2) Transmission Lines

A Clinic team proposes to drive a 45 cm wire on a printed circuit board connecting the output buffer of one chip to the input buffer of a second chip. The PCB wire has a 50 Ω characteristic impedance and a velocity of half the speed of light. Each buffer has a 5 Ω effective output impedance and an 100 MΩ effective input impedance. The buffers use LVCMOS signaling described in Table 1.4. The first buffer switches from 0 to VDD at time 0.

(a) Draw a model of the circuit similar to Figure A.19.
(b) What is the steady state voltage at the input of the second chip?
(c) Plot the voltages at the input of the second chip vs. time for the duration of interesting behavior.
(d) If the signal serves as the clock input of the second chip, what might go wrong?
(e) If the signal serves as a data input to the second chip, what might go wrong?
(f) How could the Clinic team avoid these problems?

3) Time

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for next semester's class.