Outline

- Variation
- Noise Budgets
- Reliability
- Circuit Pitfalls
Variation

- Process
  - Threshold
  - Channel length
  - Interconnect dimensions
- Environment
  - Voltage
  - Temperature
- Aging / Wearout
Process Variation

- Threshold Voltage
  - Depends on placement of dopants in channel
  - Standard deviation inversely proportional to channel area
    \[ \sigma_{V_t} = \frac{t_{ox}}{e_{ox}} \sqrt{\frac{q^3 \epsilon_{ox} \phi_p N_d}{\sqrt{2LW}}} = \frac{A_{V_t}}{\sqrt{LW}} \]

- Channel Length
  - Systematic across-chip linewidth variation (ACLV)
  - Random line edge roughness (LER)

- Interconnect
  - Etching variations affect \( w, s, h \)

Courtesy Texas Instruments

[ Bernstein06 ]

[ Bernstein06 ]
Spatial Distribution

- Variations show spatial correlation
  - Lot-to-lot (L2L)
  - Wafer-to-wafer (W2W)
  - Die-to-die (D2D) / inter-die
  - Within-die (WID) / intradie
- Closer transistors match better

Courtesy M. Pelgrom
Environmental Variation

- **Voltage**
  - $V_{DD}$ is usually designed +/- 10%
  - Regulator error
  - On-chip droop from switching activity

- **Temperature**
  - Ambient temperature ranges
  - On-die temperature elevated by chip power consumption

<table>
<thead>
<tr>
<th>Standard</th>
<th>Minimum</th>
<th>Maximum</th>
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<tbody>
<tr>
<td>Commercial</td>
<td>0 °C</td>
<td>70 °C</td>
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<tr>
<td>Industrial</td>
<td>-40 °C</td>
<td>85 °C</td>
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<tr>
<td>Military</td>
<td>-55 °C</td>
<td>125 °C</td>
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</table>

[Courtesy IBM][Harris01b]
Aging

- Transistors change over time as they wear out
  - Hot carriers
  - Negative bias temperature instability
  - Time-dependent dielectric breakdown
- Causes threshold voltage changes
- More on this later…
Process Corners

- Model extremes of process variations in simulation
- Corners
  - Typical (T)
  - Fast (F)
  - Slow (S)
- Factors
  - nMOS speed
  - pMOS speed
  - Wire
  - Voltage
  - Temperature

<table>
<thead>
<tr>
<th>Corner</th>
<th>Voltage</th>
<th>Temperature</th>
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<tr>
<td>F</td>
<td>1.98</td>
<td>0 °C</td>
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<tr>
<td>T</td>
<td>1.8</td>
<td>70 °C</td>
</tr>
<tr>
<td>S</td>
<td>1.62</td>
<td>125 °C</td>
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## Corner Checks

- Circuits are simulated in different corners to verify different performance and correctness specifications

<table>
<thead>
<tr>
<th>Corner</th>
<th>nMOS</th>
<th>pMOS</th>
<th>Wire</th>
<th>$V_{DD}$</th>
<th>Temp</th>
<th>Purpose</th>
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<td>S</td>
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<td>Races of gates against wires</td>
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<td>T</td>
<td>F</td>
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<td>Pseudo-nMOS and ratioed circuits noise margins, memory read/write, race of pMOS against nMOS</td>
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<td>F</td>
<td>F</td>
<td>Ratioed circuits, memory read/write, race of nMOS against pMOS</td>
</tr>
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</table>
Monte Carlo Simulation

- As process variation increases, the worst-case corners become too pessimistic for practical design
- Monte Carlo: repeated simulations with parameters randomly varied each time
- Look at scatter plot of results to predict yield
- Ex: impact of $V_t$ variation
  - ON-current
  - leakage
Noise

- Sources
  - Power supply noise / ground bounce
  - Capacitive coupling
  - Charge sharing
  - Leakage
  - Noise feedthrough
- Consequences
  - Increased delay (for noise to settle out)
  - Or incorrect computations
Reliability

- Hard Errors
  - Oxide wearout
  - Interconnect wearout
  - Overvoltage failure
  - Latchup
- Soft Errors
- Characterizing reliability
  - Mean time between failures (MTBF)
    • # of devices \times hours of operation / number of failures
  - Failures in time (FIT)
    • # of failures / thousand hours / million devices
Accelerated Lifetime Testing

- Expected reliability typically exceeds 10 years
- But products come to market in 1-2 years
- Accelerated lifetime testing required to predict adequate long-term reliability

[Graph showing DC Lifetime 10% ion [Hrs] vs. Vdd stress [Volt]]

[Source: Arnaud08]
Hot Carriers

- Electric fields across channel impart high energies to some carriers
  - These “hot” carriers may be blasted into the gate oxide where they become trapped
  - Accumulation of charge in oxide causes shift in $V_t$ over time
  - Eventually $V_t$ shifts too far for devices to operate correctly
- Choose $V_{DD}$ to achieve reasonable product lifetime
  - Worst problems for inverters and NORs with slow input risetime and long propagation delays
NBTI

- Negative bias temperature instability
- Electric field applied across oxide forms dangling bonds called traps at Si-SiO₂ interface
- Accumulation of traps causes $V_t$ shift
- Most pronounced for pMOS transistors with strong negative bias ($V_g = 0, V_s = V_{DD}$) at high temperature

$$\Delta V_t = k e \frac{E_{ox}}{E_0} t^{0.25}$$

$$E_{ox} = V_{DD}/t_{ox}$$
TDDB

- *Time-dependent dielectric breakdown*
  - Gradual increase in gate leakage when an electric field is applied across an oxide
  - a.k.a *stress-induced leakage current*
- For 10-year life at 125 C, keep $E_{ox}$ below $\sim 0.7$ V/nm
Electromigration

- "Electron wind" causes movement of metal atoms along wires
- Excessive electromigration leads to open circuits
- Most significant for unidirectional (DC) current
  - Depends on current density $J_{dc}$ (current / area)
  - Exponential dependence on temperature
  - Black’s Equation: $MTTF \propto \frac{e^{\frac{E_a}{kT}}}{J_{dc}^n}$
  - Typical limits: $J_{dc} < 1 – 2$ mA / $\mu$m²

[Christiansen06]
Electromigration Video
In-situ Observation of Electromigration via HVSEM

J. Doan, S. Lee J. Bravman, P. Flinn, *T. Marieb

Dept. of Materials Science & Engineering, Stanford University
*Components Research, Intel Corporation - Santa Clara

Aluminum Alloy Study: Alsctnt01
1/19/97

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Self-Heating

- Current through wire resistance generates heat
  - Oxide surrounding wires is a thermal insulator
  - Heat tends to build up in wires
  - Hotter wires are more resistive, slower
- Self-heating limits AC current densities for reliability

\[
I_{\text{rms}} = \sqrt{\frac{\int_0^T I(t)^2 \, dt}{T}}
\]

- Typical limits: \( J_{\text{rms}} < 15 \text{ mA} / \mu \text{m}^2 \)
Overvoltage Failure

- High voltages can blow out tiny transistors
- Electrostatic discharge (ESD)
  - kilovolts from static electricity when the package pins are handled
- Oxide breakdown
  - In a 65 nm process, $V_g \approx 3$ V causes arcing through thin gate oxides
- Punchthrough
  - High $V_{ds}$ causes depletion region between source and drain to touch, leading to high current flow and destructive overheating
Latchup

- Latchup: positive feedback leading to $V_{DD} - GND$ short
  - Major problem for 1970’s CMOS processes before it was well understood
- Avoid by minimizing resistance of body to GND / $V_{DD}$
  - Use plenty of substrate and well taps
Guard Rings

- Latchup risk greatest when diffusion-to-substrate diodes could become forward-biased
- Surround sensitive region with guard ring to collect injected charge
In 1970’s, DRAMs were observed to randomly flip bits
- Ultimately linked to alpha particles and cosmic ray neutrons
Collisions with atoms create electron-hole pairs in substrate
- These carriers are collected on p-n junctions, disturbing the voltage

[Baumann05]
Radiation Hardening

- Radiation hardening reduces soft errors
  - Increase node capacitance to minimize impact of collected charge
  - Or use redundancy
  - E.g. dual-interlocked cell

- Error-correcting codes
  - Correct for soft errors that do occur
Detective puzzle
- Given circuit and symptom, diagnose cause and recommend solution
- All these pitfalls have caused failures in real chips
Bad Circuit 1

- **Circuit**
  - 2:1 multiplexer

- **Symptom**
  - Mux works when selected D is 0 but not 1.
  - Or fails at low $V_{DD}$.
  - Or fails in SFSF corner.

- **Principle:**
  - X never rises above $V_{DD} - V_t$
  - $V_t$ is raised by the body effect
  - The threshold drop is most serious as $V_t$ becomes a greater fraction of $V_{DD}$.

- **Solution:**
  - Use transmission gates, not pass transistors
Bad Circuit 2

- Circuit
  - Latch

- Symptom
  - Load a 0 into Q
  - Set $\phi = 0$
  - Eventually Q spontaneously flips to 1

- Principle:
  - 
  - 

- Solution:
Bad Circuit 3

☐ Circuit
  – Domino AND gate

☐ Symptom
  – Precharge gate (Y=0)
  – Then evaluate
  – Eventually Y spontaneously flips to 1

☐ Principle:
  – 
  – 

☐ Solution:
Bad Circuit 4

- **Circuit**
  - Pseudo-nMOS OR

- **Symptom**
  - When only one input is true, \( Y = 0 \).
  - Perhaps only happens in SF corner.

- **Principle:**
  - 
  - 

- **Solution:**
Bad Circuit 5

- **Circuit**
  - Latch

  \[ \text{D} \xrightarrow{\phi} \times \xrightarrow{\text{weak}} \text{Q} \]

- **Symptom**
  - Q stuck at 1.
  - May only happen for certain latches where input is driven by a small gate located far away.

- **Principle:**

- **Solutions:**

- Check relative strengths
- Avoid unbuffered diffusion inputs where driver is unknown
**Bad Circuit 6**

- **Circuit**
  - Domino AND gate

- **Symptom**
  - Precharge gate while $A = B = 0$, so $Z = 0$
  - Set $\phi = 1$
  - $A$ rises
  - $Z$ is observed to sometimes rise

- **Principle:**
  - Charge Sharing
  - If $X$ was low, it shares charge with $Y$

- **Solutions:**
  - Limit charge sharing
  - Safe if $C_Y > C_X$
  - Or precharge node $X$ too
Bad Circuit 7

- Circuit
  - Dynamic gate + latch

- Symptom
  - Precharge gate while transmission gate latch is opaque
  - Evaluate
  - When latch becomes transparent, X falls

- Principle:

- Solution:
Bad Circuit 8

- Circuit
  - Latch

- Symptom
  - Q changes while latch is opaque
  - Especially if D comes from a far-away driver

- Principle:
  -
  -

- Solution:
Summary

- Static CMOS gates are very robust
  - Will settle to correct value if you wait long enough
- Other circuits suffer from a variety of pitfalls
  - Tradeoff between performance & robustness
- Essential to check circuits for pitfalls
  - For large chips, you need an automatic checker.
  - Design rules aren’t worth the paper they are printed on unless you back them up with a tool.