E158 Project 2 Rubric

Designers:
Chip:

Proposal: __ / 10

Verilog __ / 15
 Test bench demonstrates functions specified in proposal __ / 5
 Passes self-checking test bench __ / 5
 Suitable for conversion to schematics __ / 3
 Readable / commented __ / 2

Schematic __ / 10
 At least one custom leaf cell __ / 2
 At least one custom block __ / 3
 At least one synthesized block __ / 1
 Pad frame __ / 1
 Passes self-checking test-bench __ / 3
 Analog blocks simulate in SPICE (if applicable) __ / + 1

Block Layout __ / 5
 Leaf cell drawn cleanly __ / 1
 Synthesized block layout __ / 1
 Custom block > 50% complete & clean __ / 1
 DRC __ / 1
 LVS __ / 1

Final Project __ / 30
 All layouts complete __ / 5
 Pass DRC (no join nets) __ / 7
 Pass LVS (no join nets) __ / 7
 Schematics still pass test bench __ / 5
 Core routed to pad frame __ / 3
 CIF reads back and passes DRC & LVS __ / 3

Report __ / 20
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 Specifications __ / 2
 Floorplan __ / 4
 Verification __ / 2
 Postfabrication test plan (if applicable) __ / +2
 Design Time __ / 2
 File Locations __ / 2
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