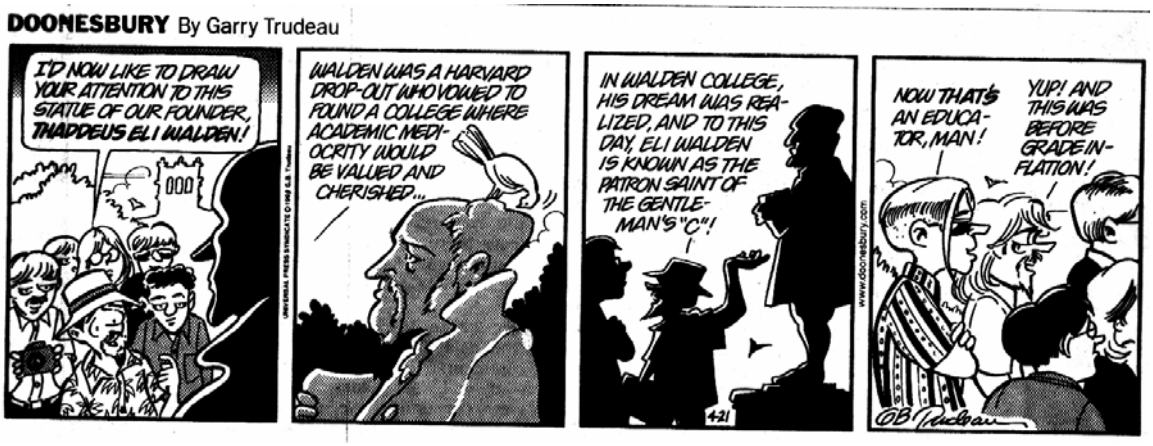
Harris

Introduction to CMOS VLSI Design (E158)

Problem Set 5



The objective of this problem set is to learn to use HSPICE to predict the delay and power consumption of circuits.

To invoke HSPICE, type `hspice deck.sp > deck.lis`. This will simulate `deck.sp` and write the results to a file named `deck.lis` that you can examine by typing `more deck.lis` or `gedit deck.lis`. To look at the results in SPICE Explorer, make sure your deck includes a .option post statement. After simulation, type `sx`. Then import the waveform file (e.g. deck.tr0 for a transient simulation).

1) Inverter Delay Simulation

This problem explores how the delay of an inverter varies with fanout. Copy the fo4.sp SPICE deck from /courses/e158/10/ps5 to a new ps5 directory in your home directory.

(a) Run an HSPICE simulation on fo4.sp and determine the rising, falling, and average delay of a fanout-of-4 inverter at 3.3 V and 70 ºC (the standard simulation conditions for this course unless specified otherwise).

(b) Make a plot of the input and output waveforms for the inverter device under test using Spice Explorer. Open fo4.tr0 and look at the c and d waveforms. Measure the rising and falling delays using Tools • Measurement. Under the All Tab, choose Time Domain and then in the Measurement field choose Delay. Set the Delay to measure from signal level of 1.65 to reference level 1.65 ($V_{DD}/2$). Do they match the results from part (a)?

To print your waveforms, first choose Config • Preferences to set up the printers. In the Printer Devices field, enter c3p0;r2d2;StarDestroyer. Then choose File • Print. The printer will default to c3po, the color printer in the ECF.

(c) Comment out the two lines specifying the areas and perimeters of the source and drain of each transistor. Rerun the simulation and find the average delay. How much does it change? Why is it important to accurately include these parasitics?

(d) The simulation setup involves 5 inverters, which seems like it might be unnecessarily complicated to determine the delay of a single inverter. Modify the simulation to have a single inverter driving a load of H inverters. Rerun your simulation. How much does the average delay change? Why is it important to include the chain of 5 gates?

(e) Change the .tran statement in the original deck to

```
.tran 5ps 10000ps SWEEP H 1 8 1
```

to sweep over multiple simulations with fanouts (H) from 1 to 8 in steps of 1. Graph your average delay vs. fanout using Excel, Matlab, or your other favorite plotting program. Determine the equation of the line that best fits $d = (h + p)\,\tau$, where d is delay in picoseconds and h is the fanout. τ should have units of picoseconds, while h and p are dimensionless. What is the maximum percentage error of your curve fit vs. the data? If you hope to achieve accuracies of 10%, is this curve fit a good way to predict inverter delay? Give a physical explanation of why the model is reasonable or not.

2) Inverter Noise Margins

Simulate the DC transfer characteristics of the inverter from problem 1. Look at the results in Spice Explorer and determine the logic levels: V_{IH}, V_{IL}, V_{OH}, and V_{OL}. What is the worst-case noise margin of the gate?

3) Path Optimization

This problem explores the energy and delay tradeoffs of a circuit and the relationship between hand calculations and simulation results.

(a) Revisit Problem 3 from Problem Set 4, using simulation. Simulate the design that you concluded would give the minimum energy-delay product. What sizes did you select? What are the energy, delay, and EDP for these sizes? Let a unit inverter have a 4 λ nMOS and an 8 λ pMOS. Use an input with a 300 ps transition time. Don't bother to shape the input or place a load on the load. Be sure to connect the appropriate power supplies so that you measure the energy of only the intended components.

(b) Tune your design in simulation and see if you can improve the EDP. Hint: use SWEEP to vary the width of one buffer at a time. What are the new sizes that give best results and how much better are the results? Were your hand calculations sufficient to give a good design, or was tuning in simulation necessary to get satisfactory results?

4) Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for the future.