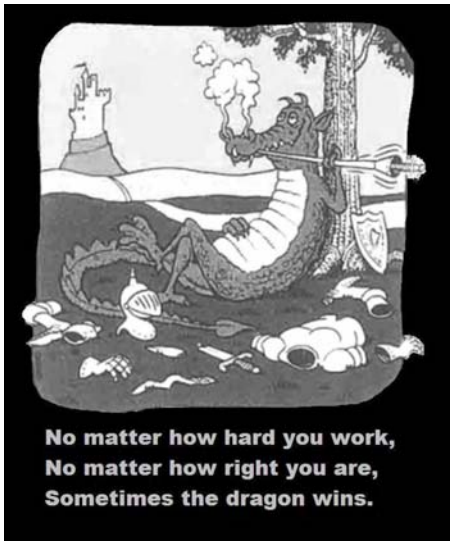
Introduction to CMOS VLSI Design (E158)

Problem Set 4

Harris

1) Power in a Gate



Consider the AOI gate from Problem Set 3 sized for the same drive as a unit inverter (4 λ nMOS, 8 λ pMOS). The AOI drives 4 unit inverters and 300 λ of wire. New inputs are applied every cycle with a 100 MHz clock. Each input has an equal chance of being 0 or 1. Your 0.6 μm process operates at 3.3 V and has gate and diffusion capacitance of 2 fF/μm and a wire capacitance of 0.2 fF/μm. Estimate the dynamic power consumption of the circuit. Account for the load and for internal parasitics on the output node, but not the input capacitance (which draws power from a previous stage).

2) Leakage Power

Assume that nMOS and pMOS transistors have equal subthreshold leakage per unit width and that other forms of leakage are negligible. When two series transistors are both off, assume the stack effect reduces leakage by a factor of 10. For what value of I_{off} would the leakage power equal half of the dynamic power in the AOI?

3) Energy-Delay Product

A controller contains a unit inverter producing an output signal. The signal must drive 64 unit-sized loads in a datapath. You may add any number of stages of inverters to buffer the signal; the polarity is not important. If your goal is to minimize the energy-delay product, how many stages should you add and how wide should each stage be?

4) Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for the future.