Harris

Introduction to CMOS VLSI Design (E158)

Syllabus

Spring 2008

Teaching Staff

Professor: David Money Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: TuTh 2:45 – 4:00
Office Hours: TBD
Design Reviews: Wednesday 7:30-10:30 PM

Feel free to stop by even if I do not have official office hours.

Texts

CMOS VLSI Design, 3rd Ed., (Weste & Harris, Addison-Wesley, 2005) is the primary text. I will be starting the 4th edition and would welcome constructive criticism to improve the book. I also pay a bounty for the first person to report each bug in the book.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158

Grading

Labs:	10%
Problem Sets:	10%
In-class Activities:	5%
Project 1:	20%
Project 2:	40%
Midterm:	15%

The emphasis of this class is hands-on chip design. During the first four weeks, you will complete a series of labs to build an 8-bit MIPS microprocessor. Along the way, you will master a variety of CAD tools and design techniques.

Labs and problem sets are due by the end of class and will not be graded if submitted late. However, the labs build toward assembly of the entire processor, so it is important not to fall behind. Your lowest problem set and two activity scores will be dropped before the average is calculated; if you need to miss more classes because of interviews or illness, contact Prof. Harris. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work or refer to solutions from previous years.**

There are two projects this year. The first is to build a 20-bit adder optimized for energy and delay. You will work by yourself on this project to explore designing a subsystem of moderate complexity. The second is to design an entire chip. You will work in team to explore partitioning the large system. This year's chip is a 6502 microprocessor, which is the brain of the Apple II and Commodore 64 computers. We will fabricate the chip and test it in a real computer next fall.

You may be able to find solutions to in class activities or problem sets on the Web or in past student archives. It should go without saying that using any such materials or doing anything to gain an unfair advantage over your classmates is an honor code violation.

Tentative Schedule

The attached schedule is a tentative plan that probably will change during the semester. The schedule lists reading associated with each lecture. You are expected to do the reading before class and be prepared to discuss it. However, you may skip over advanced sections marked with a black square.

00000	22-Jan	Introduction and overview	1.1-1.4	
00001	24-Jan	Circuits and layout	1.5	
00010	29-Jan	Design flow	1.6-1.12	Lab 1: Cell Design
00011	31-Jan	Circuit simulation	5.1	PS 1: Schematics & Sticks
00100	5-Feb	-- Silicon Run Video --		Lab 2: Datapath Design
00101	7-Feb	CMOS transistor theory	2.1-2.2	PS 2: Simulation
00110	12-Feb	DC and transient response	2.5	Lab 3: Control Design
00111	14-Feb	Logical Effort	4.1-4.3	Proj 1A: Adder RTL
	19-Feb	Power and interconnect	4.4-4.6	Lab 4: Chip Assembly
01000	21-Feb	Combinational circuit design	6.1-6.2.1	Proj 1B: Adder Schematics
01001	26-Feb	Clocking and latching	7.1-7.2, 7.4	PS 3: Logical Effort
01010	28-Feb	6502 microprocessor overview		Proj 1C: Adder Optimization
01011	4-Mar	Adder design reviews		
01100	6-Mar	Adder design reviews		Proj 2A: Block Schematics
01101	11-Mar	Circuit families	6.2.2-6.2.5	
01110	13-Mar	Sequential circuit design	7.3	Proj 2B: Chip Schematics
	18-Mar	-- Spring Break: No Class --		
	20-Mar	-- Spring Break: No Class --		
01111	25-Mar	Midterm Review	10.2	
10000	27-Mar	Midterm	10.3-10.9	
10001	1-Apr	Nonideal transistor characteristics	2.4	
10010	3-Mar	Low power design	6.5	Proj 2C: Optimization
10011	8-Apr	Circuit pitfalls	6.3, 4.7-4.8	
10100	10-Apr	Design for testability	9.1, 9.6-9.7	Proj 2D: Block Layout
10101	15-Apr	Adders	10.2	
10110	17-Apr	Datapath circuit design	10.3-10.9	Proj 2E: Chip Layout
10111	22-Apr	Arrays: SRAM	11.2	
11000	24-Apr	Arrays: ROM, PLAs	11.3-11.4	Project Report Due
11001	29-Apr	Scaling and economics	4.9	
11010	1-May	A History of Intel Microprocessor Chips		PS 4: Chip testing

Note: Final project presentations will take place during presentation days (Wednesday May 7).