The E158 class will all collaborate to build a 6502 microprocessor optimized for minimum power at 1 MHz operation. The processor will be pin-compatible with an ordinary 6502 so that it can be placed in an Apple II motherboard. It will dedicate two previously unused pins to support a lower-voltage core operation (to save power) and an error signal from a novel Razor latch.

The project will be jointly led by Nathaniel Pinckney, Chief Circuit Designer, and Thomas Barr, Chief Microarchitect. The microarchitecture and ROM teams will report to the Chief Microarchitect, while the Schematic & Optimization, Physical Design, I/O, and Clocking teams will report to the Chief Circuit Designer.

This document defines the project deliverables. All deliverables are due at the Wednesday evening design reviews. At each review, turn in a document demonstrating that the milestones have been achieved. This could take the form of schematics, layout, SPICE graphs, Java code, a written statement about verification status, or so forth, depending on the specific milestone. The milestones are likely to be revised at least once during the project. Please provide prompt feedback if you see unrealistic objectives.

The design reviews will take place in the VLSI War Room (Parsons 2383, a.k.a the MicroP’s Lab).

Your project grade will be based on the following factors:

- Weekly written deliverable reports: 25%
- Quality of deliverables based on review: 25%
- On-time completion of milestones: 25%
- Project Report: 15%
- Self and Peer Evaluations: 5%
- Presentations Days Presentation: 5%

Satisfactory completion of your initially assigned objectives will earn a B for the project. Unforseen milestones will inevitably arise. You can raise your grade by a letter by taking on some of these tasks or by volunteering to be a team leader.
WW 1 (5 March)

Schematic Team + Physical Design Team

Schematics simulate in ModelSim with testfixtures and testvectors made by designers.

branchlogic
mux5_1x
regbit  (fig 1.13a)
regbitbuf
latch_dp_1x
latchr_dp_1x
latchen_dp_1x
mux5_1x_8
inc_8
regfile_8
registerbuf_8, registerbufmasked_8
alu_8
latch_1x_8
latchr_1x_8
latchen_1x_8

The performance of the inc_8 and alu_8 will be important to the chip’s overall performance, so these should be optimized.

I/O
Schematics simulate in ModelSim with testfixtures and testvectors made by designers.
levelconv_1x  (12.25a) pad_out lc, pad_inout lc

Razor
Schematics simulate in ModelSim with testfixtures and testvectors made by designers.
razorlatch_dp_1x (see notes) razorrach_1x_8

Microarchitecture (Microarchitects)

RTL Rev 1(Barr)
Pass regression suites A and B
ROM contents may not be able to boot Apple II
RTL rearranged to match planned hierarchy
ROMs retimed into half cycles
Critical path analysis
Delays in modules
Razor in RTL, analyze hold time risks

Regression Suite A: Tests all instructions (passes in RTL and match emulator)
Regression Suite P: ~10 instructions for testing power
Self-checking test benches

ROM Generation:
The ROM generator should parse a case statement in the same format as is expected by the PLA generator. Or better yet, it could read a Verilog module with inputs and outputs and a single case statement, Then generate a ROM with the appropriately named I/Os. The ROM format should match Figure 11.39. Use 3/3 λ pseudo-nMOS pullups and 4/2 λ transistors in the array. Use 4x inverters on the output and appropriately sized inverters and buffers on the address inputs.

WW1 deliverables:
parse case statement similar to PLA generator
Emit layout of at least one component of the ROM
WW 2 (12 March)

**Schematic and Optimization**
- Chip schematics complete
- Chip passes regression suite A
  - datapath
  - controller latches and other hardware as needed
  - controller
  - core
  - chip (based on pad frame generator)

**Physical Design**
- Cell layout
- pass DRC, ERC, NCC
- mux8_1x
- mux5_1x
- halfadder
- regbit
- regbitbuf
- alu
- latch_dp_1x
- latched_dp_1x
- latcheden_dp_1x

**ROM Generation:**
- generate layout (not necessarily DRC clean or properly sized inverters)
- autogen schematic from layout
- correct simulation in Verilog
  - opcoderom
  - fsmrom
- deliver in time for full-chip integration

**I/O**
- Layout pass ERC, DRC, NCC for
  - levelconv_1x
- Write `.arr` file matching 6502 pinout plus two extras
  - pin 35 for corevdd
  - pin 36 for ERR from Razor
- Generate chip{sch} from core{sch} and pads
- Characterize level converters in HSPICE
  - DC transfer characteristics

**Microarchitecture**
- VCD files for suite A and P on chip module

**Razor**
- Layout pass ERC, DRC, NCC for
  - razorlatch_dp_1x
- Complete error detection logic schematics
- Plan Razor study
- Schematics for clocking system
**WW 3 (2 April)**

**Schematic and Optimization**
- Use vcd2sp to generate stimulus file
- Work out reasonable timing for external memory
- Simulate chip{sch} in HSPICE using Suite P
- Plot power vs. $V_{DD}$
- Determine minimum operating voltage at 1 MHz
- Make pie chart of major power consumption (ROMs, control, dp, pads)
  - Assume output pads drive 10 pF each

**Physical Design**
- Wordlib layout
- pass DRC, ERC, NCC
- mux5_1x_8
- inc_8
- regfile_8
- registerbuf_8, registerbufmasked_8
- alu_8
- latch_1x_8
- latchr_1x_8
- latchen_1x_8
- pad_out_lc, pad_inout_lc (I/O)

**ROM Generation:**
- DRC, ERC, NCC, simulate in Verilog
- SPICE characterization: output $V_{OL}$, static power consumption

**Regression Suites (Microarchitects)**
- Suite R: Boot Apple II ROM
- RTL Rev 2 passes suite R

**I/O**
- use vcd2sim to generate IRSIM test vectors from Suite P
- Simulate core{sch} in IRSIM

**Razor**
- razolatch_1x_8 layout pass DRC, ERC, NCC
- Complete physical design of Razor hardware
- Mindelay and glitch analysis
WW 4 (9 April)

**Schematic and Optimization**
Tune schematic to use less power 😊

**Physical Design**
- Unit layout
- pass DRC, ERC, NCC
- datapath
- controller latches as needed
- controller

**ROM Generation:**
Regenerate ROMs based on RTL Rev 2

**I/O**
- Use vcd2sim to generate IRSIM test vectors from Suite R
- Simulate core{sch} in IRSIM on Suite R
- Write post-fabrication test plan
  - Describes exact steps to use and equipment needed to test the chip when it returns from the fab. This should involve both functional testing on TestosterICs and in-situ testing in an Apple II. It should also describe what data should be measured and how to obtain it.

**Razor**
- Demonstrate Razor generating ERR before failure in SPICE
- Use Suite P
- Characterize detection window width (in terms of \( V_{DD} \) margin from point of ERR to point of failure)
- Demonstrate SER detection of event in combinational logic

**Microarchitecture**
- Begin ISSCC Student Design Contest 6-page paper
**WW 5 (16 April)**

**Schematic and Optimization**
Assist with ECOs for layout changes based on tuning

**Physical Design**
Completed chip layout  
Update layout to reflect schematic tuning ECOs  
pass DRC, ERC, NCC according to Lab 4 instructions  
Layout simulates suite A, R in Verilogs  
Generate CIF and record checksum  
Deliver early enough for simulation teams to finish their jobs

```
core
chip
```

**Chip Report**
Microarchitects, ROM, I/O, Razor teams begin draft

**WW 6 (23 April)**

**Chip Report**
Attractive cover page with chip plot  
Paper on Razor application to the chip  
ISSCC Student Design Contest 6-page paper  
Report outline TBD

**Schematic and Optimization**
Repeat power characterization on extracted full-chip layout

**I/O**
Simulate core{lay} in IRSIM for Suite P

**Evaluations**
Thoughtful evaluation of self and of teammates. Constructive suggestions for future improvement.

**WW 7 (7 May)**

Presentation of 6502 chip at Presentations Days