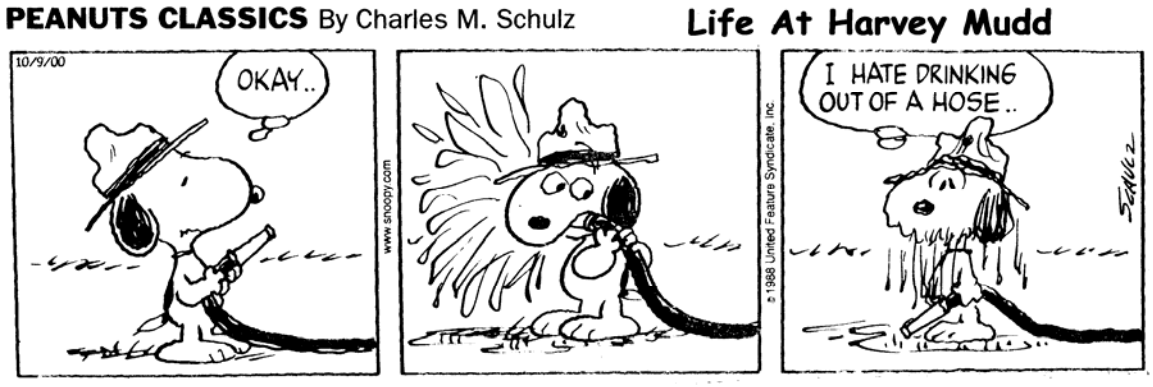
Harris

Introduction to CMOS VLSI Design (E158)

Problem Set 3

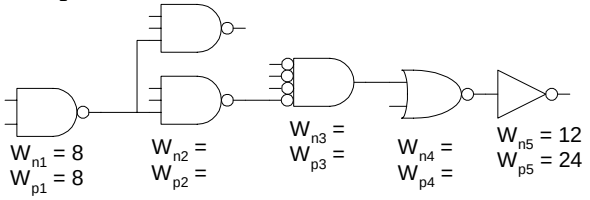


1. Consider the AOI gate from Problem Set 1. What are the transistor widths that achieve worst-case rise and fall resistance equivalent to a unit inverter. What is the logical effort of each input (hint: they are not all the same).

2. How do the logical effort and parasitic delay of the NOR gate from Problem 2b of Problem Set 2 compare to the theoretical numbers derived in class?

3. Use logical effort to predict the size h that gives lowest delay in the buffer in Problem 3a of Problem Set 2. Use the conversion that 1 micron of transistor width has approximately 2 fF of gate capacitance. How does the theory compare with your simulation results?

4. Estimate the minimum delay (in ps) of the following circuit (from NAND2 inputs switching to the NOR2 output driving the load inverter), and choose transistor widths for the nMOS and pMOS transitors that achieve this minimum delay. Use the value of τ that you found in Problem Set 2. Assume both NAND3 gates are equal size at the fork in the path.



5. Do problem 4.13 from *CMOS VLSI Design*.

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for the future.