Harris

Introduction to CMOS VLSI Design (E158)

Problem Set 2

The objective of this problem set is to learn to use HSPICE to predict the delay and power consumption of circuits.

1) This problem explores how the delay of an inverter varies with fanout. The fo4.sp SPICE deck and the 0.5 μm process models are in the E158 directory on Charlie\Courses\Engineering\Fall08\PS2.

(a) Run an HSPICE simulation and determine the rising, falling, and average delay of a fanout-of-4 inverter at 5 V and 70 C (the standard simulation conditions for this course unless specified otherwise).

(b) Make a plot of the input and output waveforms for the inverter device under test using CosmosScope. Measure the rising and falling delays using the Delay option under Time Domain measurements. Do they match the results from part (a)?

(c) Comment out the two lines specifying the areas and perimeters of the source and drain of each transistor. Rerun the simulation and find the average delay. How much does it change? Why is it important to accurately include these parasitics?

(d) The simulation setup involves 5 inverters, which seems like it might be unnecessarily complicated to determine the delay of a single inverter. Modify the simulation to have a single inverter driving a load of H inverters. Rerun your simulation. How much does the average delay change? Why is it important to include the chain of 5 gates?

(e) Change the .tran statement in the original deck to

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.tran 5ps 10000ps SWEEP H 1 8 1
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to sweep over multiple simulations with fanouts (H) from 1 to 8 in steps of 1. Graph your average delay vs. fanout using Excel, Matlab, or your other favorite plotting program. Determine the equation of the line that best fits $d = (h + p)\,\tau$, where d is delay in picoseconds and h is the fanout. τ should have units of picoseconds, while h and p are dimensionless. What is the maximum percentage error of your curve fit vs. the data? If you hope to achieve accuracies of 10%, is this curve fit a good way to predict inverter delay? Give a physical explanation of why the model is reasonable or not.

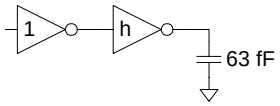
2) This problem explores the delay of a 2-input NOR gate.

(a) Write a SPICE deck to determine the average delay of a 2-input NOR gate from the A (outer) input. The deck should be similar to the one for the FO4 inverter, including a chain of 5 gates with appropriate source and drain parasitics. Turn in a printout of your deck.

(b) Graph delay vs. fanout for the NOR gate over the range of 1 to 8. Determine the equation of the line that best fits $d = (g_{nand}h + p_{nand})\,\tau$, using the value of τ from part 1(e). What is the maximum percentage error of your curve fit vs. the data? Is this equation a good way to predict NOR gate delay?

3) This problem explores the energy and delay tradeoffs of a circuit.

(a) The circuit below is a buffer driving a large capacitive load. Simulate it in HSPICE. The first inverter is unit size (e.g. 8 λ pMOS and 4 λ nMOS). The second inverter is *h* times unit size. Sweep *h* and measure the energy drawn from V_{DD} over a rising and falling transition and the average delay of the buffer. What value of *h* gives the lowest delay?



(b) Compute the energy consumed by charging and discharging the capacitor. This is called the load energy.

(c) The circuit energy is the total energy minus the load energy. Plot circuit delay vs. energy.

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for the future.