Harris

Introduction to CMOS VLSI Design (E158)

Syllabus

Spring 2007

Teaching Staff

Professor: David Money Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: TuTh 9:35-10:50
Office Hours: TBD
Design Reviews: Tuesday 7:30-10:30 PM

Feel free to stop by even if I do not have official office hours.

Texts

CMOS VLSI Design, 3rd Ed., (Weste & Harris, Addison-Wesley, 2005) is the primary text. I will be starting the 4th edition and would welcome constructive criticism to improve the book. I also pay a bounty for the first person to report each bug in the book.

The pipelined MIPS processor is described in Digital *Design and Computer Architecture* (Harris & Harris, Morgan Kaufmann, 2007). Consider this knowledge a prerequisite to the class and get yourself up to speed if you are rusty about how it works.

See MIPS Run (Sweetman, Morgan Kaufmann, 1999) is an authoritative guide to the MIPS architecture. If you are involved with the microarchitecture or system design, you may find it helpful to buy or borrow a copy.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158

Grading

Labs:	30%
Final Project:	50%
Problem Sets:	10%
In-class Activities:	10%

The emphasis of this class is hands-on chip design. During the first five weeks, you will complete a series of labs to build a divider chip. Along the way, you will master a variety of CAD tools and design techniques.

This year, the class project is unusual. Rather than carrying out self-defined projects in teams of two, the entire class will work together to build a 32-bit MIPS processor. This will give the experience of working on a large team similar to one you might work on in industry. Responsibilities will vary widely, from HDL design to circuit design to compilers to system bring-up.

Project grading will be based on your contribution to the overall project. Satisfactorily completing a block will earn a B grade. Taking on additional responsibilities such as leading a team, assembling blocks together, or handling unplanned surprises can raise the grade to an A. If your block is not adequate to be used in the project without modification by other people, or if the block is late, your project grade will be a C or lower. The quality of your writing, reviews, and presentations can raise or lower your project grade by a half point.

As you will discover, hands-on design is extraordinarily time-intensive. It is impossible for you to apply all the knowledge you gain from this class to an actual design, so a series of problem sets will give you an opportunity to master these concepts.

Labs and problem sets are due by the end of class and will not be graded if submitted late. However, the labs build toward assembly of the entire divider, so it is important not to fall behind. Your lowest problem set and two activity scores will be dropped before the average is calculated; if you need to miss more classes because of interviews or illness, contact Prof. Harris. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work or refer to solutions from previous years.**

You may be able to find solutions to in class activities or problem sets on the Web or in past student archives. It should go without saying that using any such materials or doing anything to gain an unfair advantage over your classmates is an honor code violation.

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. The schedule lists reading associated with each lecture. You are expected to do the reading before class and be prepared to discuss it. However, you may skip over advanced sections marked with a black square.

00000	16-Jan	Introduction and overview	1.1-1.4	
00001	18-Jan	Circuits and Layout	1.5	
00010	23-Jan	Design flow	1.6-1.12	Lab 0 due
00011	25-Jan	Cell design reviews, project scheduling		PS 1 due
00100	30-Jan	CMOS transistor theory	2.1-2.2	Lab 1 due
00101	1-Feb	DC and transient response	2.5	
00110	6-Feb	Logical effort	4.1-4.3	Lab 2 due
00111	8-Feb	Delay estimation activity		PS 2 due
	13-Feb	-- Silicon Run Video --, Floorplanning activity		Lab 3 due
01000	15-Feb	Simulation	5.1-5.2, 5.5	PS 3 due
01001	20-Feb	Simulation activity		
01010	22-Feb	Combinational circuit design	6.1-6.2.1	PS 4 due
01011	27-Feb	Circuit families	6.2.2-6.2.5	
01100	1-Mar	Circuit design activity		
01101	6-Mar	Sequential circuit design	7.1-7.4	
01110	8-Mar	Interconnect engineering	4.5	PS 5 due
	13-Mar	-- Spring Break: No Class --		
	15-Mar	-- Spring Break: No Class --		
01111	20-Mar	Adders	10.2	
10000	22-Mar	Datapath Circuit Design	10.3-10.9	
10001	27-Mar	Arrays: SRAM	11.1-11.2	
10010	29-Mar	Arrays: ROM, PLAs	11.4-11.5	
10011	3-Apr	Nonideal transistor characteristics	2.4	
10100	5-Apr	TBD		
10101	10-Apr	Low Power Design	4.4, 6.5	
10110	12-Apr	Circuit Pitfalls	6.3, 4.7-4.8	
10111	17-Apr	Scaling and economics	4.9	
11000	19-Apr	Design for testability	9.1, 9.6-9.7	PS 6 due
11001	24-Apr	Packaging, I/O, & clock and power distribution	12.1-12.5	
11010	26-Apr	A History of Intel Microprocessor Chips		PS 7 due

Note: Final project presentations will take place during presentation days (Wednesday May 2).