1. Overview

The final project is a chance for you to apply your new skills in VLSI design to a moderate sized problem of your choosing as part of a two-person team. You should begin thinking about a project and teammate right away. Your project has the following milestones:

2/21:	Preliminary Project Proposal Due
2/28:	Project Proposal Due
3/9:	Floorplan Complete
3/23:	Schematics Checkoff
4/4:	Leaf Cells Complete
4/4-6:	Design Reviews
4/13:	Final Project Checkoff, Report Due
5/4:	Project Presentations

2. Project Suggestions

Be creative when selecting your project. Your project should be bigger than a weekly lab assignment, but small enough to be doable. If in doubt, err on the side of smaller; you will receive a much better grade for a simple project that is completed and convincingly verified than a large project that is incomplete.

Your project should fit on a 1.5 x 1.5 mm 40-pin MOSIS "TinyChip" fabricated in a 0.6 μm process. That means your project must not exceed 5000 x 5000 λ including I/O pads. Therefore, the core of your project must fit in a 3400 x 3400 λ box and have no more than 40 pins. Six pins should be dedicated to VDD/GND, so only 34 are available as I/Os. Exceptions may be made for project proposals that need to exceed this area or pin count but are simple enough to be feasible in the time allotted; such projects will not be placed in a pad frame. Unless negotiated in the proposal, there will be a grade penalty for exceeding the area available.

Your project should include the layout of at least two new leaf cells and some cells organized as a datapath or array; do not just synthesize a bunch of Verilog and feed it to the Silicon Compiler. Examples of suitable projects are listed below, but do not let the list limit your imagination!

- SRT Divider
- Phase-locked loop
- Metastability characterization circuit
- Process characterization circuits
- Alarm Clock
- MIPS processor with new instructions or on-chip memory
- Tiny FPGA
- Digital Signal Processing unit
- Encryption or Decryption circuitry
- Clinic-related circuits
- Games (tic-tac-toe, checkers, etc.)
- Cache memory
- Translation lookaside buffer
- Analog / Digital Converter
- CORDIC function generator
- High-speed adder

3. Design Budgeting

One of the challenges of chip design is to learn to budget your time and area. Experience is crucial to doing this well. One of the elements of the project will be to track this data so that you can learn to budget in the future.

Early in your project, you will submit a floorplan with area estimates. At the conclusion of the project, you will submit a comparison between the initial estimates and the actual results, along with an explanation of discrepancies.

Even more importantly, track the time you spend on the project. Keep a notebook and update it each day you work on the project. Note how much time you spent on each facet. Include the time spent designing the schematic, icon, and layout as well as time spent for simulation, DRC, ERC, and NCC.

4. IC Fabrication

Harvey Mudd has received funding from the MOSIS Educational Program to fabricate up to 3 TinyChip projects. If your chip is fabricated, you will receive 5 packaged parts in the fall. Priority for fabrication will be given to teams on the following basis:

1. Layout fits on a 40-pin MOSIS Tiny Chip and is wired to the pad frame provided.
2. Layout passes all DRC, ERC, and NCC tests and simulates successfully
3. At least one teammate is on campus in the fall and is committed to testing the chip.
4. Among teams meeting the above qualifications, the teams receiving the highest grades will have priority to fabricate.

5. Deliverables

Your team is responsible for the following deliverables on the dates described above:

Project Proposal

A 2-page proposal describing what you plan to build. It must be specific enough that the instructor can determine when you demonstrate your project that it meets the specs of the proposal. The proposal should also include a table listing all the inputs, outputs, and bidirectional pins on the chip.

Floorplan Complete

A brief report describing the facets used in the design and the chip floorplan. It should list every facet that will be used in the design and the estimated areas of each facet. State the number of unique leaf cells that must be drawn. The floorplan should show how the overall chip will be partitioned into major units and how the units will be physically arranged. All of the interconnections between these units should also be specified. See Section 1.10.1 for an example of a floorplan.

Schematic Checkoff

Schedule a checkoff with the instructor to demonstrate that the schematics are complete and simulate successfully at the top level. Be sure that your simulations demonstrate complete operation of the functionality specified in the proposal.

Leaf Cells Complete

A brief report listing each leaf cell in the design. With each cell, compare the actual cell area to the estimate from the floorplan.

In-class Design Review

A presentation of your project to the class for review. Begin with an overview of the project including a functional description, block diagram, inputs and outputs, and current floorplan.. Delve into the high-risk elements of the design to identify and solve problems.

Final Project Checkoff & Project Report

See separate grading sheet for expectations.

Your final report should convince the reader that your design will function and meet specifications if fabricated. It should also provide all the information another engineer would need to know to test your chip after fabrication.

Turn in a hard copy of your report. Post the following items on your E158 web page:

- PDF copy of your report
- CIF file for your chip
- IRSIM .cmd file to test your chip with the pads attached
- a ZIP archive with all of your Electric libraries

Make yourself a plot of your chip on the plotter.

Project Presentation

You will give a 10-minute conference-style presentation of your chip during presentation days. Your presentation should explain your design and results to your classmates. It should include a functional overview, the chip pinout and floor plan, simulation and verification results, design time and area budgets, performance estimates, and a top-level chip layout. The presentation should be in PowerPoint or PDF format for projection in class. Include a plot of your chip.

6. Grading

Your project will be graded as follows:

Proposal	10%
Floorplan	5%
Schematic Checkoff	10%
Leaf Cells Complete	5%
In-class Design Review	5%
Final Checkoff	30%
Final Report	25%
Presentation	10%

If you feel there has been inequity between the work you and your teammate deliver, contact the instructor.

As we all know, Electric is not a perfect tool. Keep regular backups of your project should Electric corrupt your library (very rare, but potentially very bad).