Harris

Introduction to CMOS VLSI Design (E158)

Syllabus

Spring 2004

Teaching Staff

Professor: David Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: MW 2:45-4:00
Office Hours: M 4-5, T 3-4

I am in my office more often than not, so feel free to stop by even if I do not have official office hours.

Texts

Weste & Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd ed, Addison Wesley, 2004.
Patterson & Hennessy, *Computer Organization & Design*, 2nd ed, Morgan Kaufmann, 1998.

CMOS VLSI Design is the primary text. I am in the process of coauthoring the third edition and will be handing out course notes through the semester. *Computer Organization and Design* is the E85 textbook. You will be building a MIPS processor in this class following the design in the book, so it is assumed that you have access to the book and are familiar with the MIPS assembly language from Chapter 3, ALU design from Chapter 4, and the multicycle processor microarchitecture from Chapter 5, as well as combinational logic design and finite state machine design from Appendix B. Consider this knowledge a prerequisite to the class and get yourself up to speed if you feel rusty.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158-l

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158-l

Grading

Labs:	40%
Final Project:	45%
Problem Sets:	10%
In-class Activities:	5%

The emphasis of this class is hands-on chip design. During the first six weeks, you will complete a series of labs to build your own MIPS microprocessor. Along the way, you will master a variety of CAD tools and design techniques. Based on this experience, you and a partner will propose and carry out a final project of your choosing. Projects that are fully verified may be eligible to be manufactured.

As you will discover, hands-on design is extraordinarily time-intensive. It is impossible for you to apply all the knowledge you gain from this class to an actual design, so a series of problem sets will give you an opportunity to master these concepts.

Labs and problem sets are due by the end of class and will not be graded if submitted late because solutions will be given out. However, the labs build toward assembly of the entire processor in Lab 5, so it is important not to fall behind. Your lowest lab and homework score and lowest two activities will be dropped before the average is calculated. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work or refer to solutions from previous years.**

Intercultural Chip Design

This year we are planning an experiment in intercultural chip design. You will find that major chip designs in industry are too large to be completed by a single team at a single site. Designers from across many locations and sometimes many countries must collaborate to complete the product.

We will explore these issues with a special intercultural chip design project. A few teams of HMC students will partner with teams from the Middle East Technical University (METU) in Ankara, Turkey to take on final projects. In preparation for this experiment, we will have a few special lectures on intercultural communications and collaboration.

We are fortunate to have Prof. Tayfun Akin from METU as a partner for this project. The Turkish students are electrical engineers who have completed a similar course in chip design with a smaller-scale project and who have volunteered to try this experiment. METU teaches courses in English.

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; *do not assume* that they will change just because the lecture schedule changes.

The schedule lists reading associated with each lecture. You are expected to do the reading before class and be prepared to discuss it. However, you may skip over advanced sections marked with a black square. As this is a work in progress, there are undoubtedly still errors. You can make a major contribution by catching them. I will give extra credit and credit in the preface for the first person to report errors or sections that are difficult to understand.

00000	21-Jan	Introduction and overview	1.1-1.4	
00001	26-Jan	Circuits, fabrication, and layout	1.5	
00010	28-Jan	Microprocessor example	1.6-1.13	Lab 1 due
00011	2-Feb	CMOS transistor theory	2.1-2.3	PS 1 due
00100	4-Feb	DC gate characteristics	2.5	Lab 2 due
00101	9-Feb	Delay estimation	2.6, 4.1-4.2	PS 2 due
00110	11-Feb	Logical effort	4.3	Lab 3 due
	16-Feb	-- Silicon Run Video --	3.1-3.9 (skim)	PS 3 due
00111	18-Feb	Interconnect engineering (tapeahead)	4.5-4.6	Lab 4 due
01000	23-Feb	Simulation	5.1-5.3	Preliminary prop due
01001	25-Feb	Combinational circuit design	6.1-6.2.1	Lab 5
01010	1-Mar	Circuit families	6.2.2-6.2.5	Project proposal due
01011	3-Mar	Sequential circuit design	7.1-7.3.5	PS 4 due
01100	8-Mar	Adders	10.1-10.2	
01101	10-Mar	Datapath functional units	10.3-10.9	Floorplan due
	15-Mar	-- Spring Break: No Class --		
	17-Mar	-- Spring Break: No Class --		
01110	22-Mar	Memories	11.1-11.2	
01111	24-Mar	Memories	11.5-11.7	Schematics complete
10000	29-Mar	Non-ideal transistor characteristics	2.4	PS 5 due
10001	31-Mar	Design margining and circuit pitfalls	4.7-4.8, 6.3	
10010	5-Apr	In-class design reviews		Leaf cells complete
10011	7-Apr	In-class design reviews		
10100	12-Apr	Low power design	4.4, 6.5	
10101	14-Apr	Design for testability	9.1-9.7	Final Project due
10110	19-Apr	Skew-tolerant circuit design	7.5.1-7.5.2	
10111	21-Apr	Packaging, I/O, & clock and power distribution	12.1-12.5	PS 6 due
11000	26-Apr	Scaling and economics	4.9, 8.10	
11001	28-Apr	A History of Intel Microprocessor Chips	4.11-4.12	

Note: Final project presentations will take place during presentation days May 3-5.