Harris

Introduction to CMOS VLSI Design (E158)

Syllabus

Spring 2002

Teaching Staff

Professor: David Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: MW 2:45-4:00
Office Hours: TBD

I am in my office more often than not, so feel free to stop by even if I do not have official office hours.

Texts

Course Notes (to be handed out)
Weste & Eshraghian, *Principles of CMOS VLIS Design*, 2nd Edition, Addison-Wesley, 1993.
Patterson & Hennessy, *Computer Organization & Design*, 2nd Edition Morgan Kaufmann 1998.
Sutherland, Sproull, and Harris, *Logical Effort*, Morgan Kaufmann, 1999.
Harris, *Skew-Tolerant Circuit Design*, Morgan Kaufmann, 2001.

Principles of CMOS VLSI Design is the primary text. I am in the process of coauthoring the third edition and will be handing out course notes through the semester. You should obtain a copy of the 2nd edition. You will need it for weekly readings and for reference on problem sets and labs. It is somewhat dated, but still has the best coverage of the fundamentals of any book in the field. *Computer Organization and Design* is the E85 textbook. You will be building a MIPS processor in this class following the design in the book, so it is assumed that you have access to the book and are familiar with the MIPS assembly language from Chapter 3, ALU design from Chapter 4, and the multicycle processor microarchitecture from Chapter 5, as well as combinational logic design and finite state machine design from Appendix B. Consider this knowledge a prerequisite to the class and get yourself up to speed if you feel rusty. *Logical Effort* and *Skew-Tolerant Circuit Design* are two of my favorite books and are recommended reading if you are considering graduate school or professional practice in the field of chip design.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158-l

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158-l

You also will need a computer account in the Engineering Design Center to complete your labs. If you do not have one or have forgotten your password, see a system administrator.

Grading

Labs:	40%
Final Project:	45%
Problem Sets:	10%
In-class Activities:	5%

The emphasis of this class is hands-on chip design. During the first six weeks, you will complete a series of labs to build your own MIPS microprocessor. Along the way, you will master a variety of CAD tools and design techniques. Based on this experience, you and a partner will propose and carry out a final project of your choosing. Projects that are fully verified may be eligible to be manufactured.

As you will discover, hands-on design is extraordinarily time-intensive. It is impossible for you to apply all the knowledge you gain from this class to an actual design, so a series of problem sets will give you an opportunity to master these concepts.

Labs and problem sets are due by the end of class and will not be graded if submitted late because solutions will be given out. However, the labs build toward assembly of the entire processor in Lab 5, so it is important not to fall behind. Your lowest lab and homework score will be dropped before the average is calculated. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work.**

Intercultural Chip Design

This year we are planning an experiment in intercultural chip design. You will find that major chip designs in industry are too large to be completed by a single team at a single site. Designers from across many locations and sometimes many countries must collaborate to complete the product.

We will explore these issues with a special intercultural chip design project. A few teams of HMC students will partner with teams from the Middle East Technical University (METU) in Ankara, Turkey to take on final projects. In preparation for this experiment, we will have a few special lectures on intercultural communications and collaboration.

We are fortunate to have Prof. Tayfun Akin from METU as a partner for this project and to have funding from the Mellon Foundation to get hardware to facilitate this communication. The Turkish students are electrical engineers who have completed a similar course in chip design with a smaller-scale project and who have volunteered to try this experiment. METU teaches courses in English.

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; *do not assume* that they will change just because the lecture schedule changes.

The schedule lists recommended readings with each lecture.

00000	23-Jan	Introduction and overview	WE Ch.1	
00001	28-Jan	Circuits, fabrication, and layout		
00010	30-Jan	Microprocessor example		Lab 1 due
(a)	1 Feb	Special guest lecture on Intercultural Communication		
	4-Feb	-- Intl. Solid State Circuits Conf: No Class --		PS 1 due
00011	6-Feb	CMOS transistor theory	WE 2.1-2.2	Lab 2 due
(b)	8-Feb	Special tutorial on Verilog	Verilog Tut	
00100	11-Feb	DC gate characteristics	WE 2.3-2.7	
00101	13-Feb	CMOS processing technology	WE Ch. 3	Lab 3 due
00110	18-Feb	Logical effort	Harris: LE	PS 2 due
00111	20-Feb	Interconnect engineering	WE 4.1-4.4	Lab 4 due
01000	25-Feb	Simulation	WE 6.6.1	Preliminary prop due
01001	27-Feb	Combinational circuit design	WE 5.1-5.3	Lab 5
01010	4-Mar	Circuit families	WE 5.4	Project proposal due
01011	6-Mar	Sequential circuit design	WE 5.5	
01100	11-Mar	Adders	WE 8.2.1	PS 3 due
01101	13-Mar	Datapath functional units	WE 8.2	Floorplan due
	18-Mar	-- Spring Break: No Class --		
	20-Mar	-- Spring Break: No Class --		
01110	25-Mar	Memories	WE 8.3	
01111	27-Mar	Memories		Schematics complete
10000	1-Apr	Control system design	WE 8.4	PS 4 due
10001	3-Apr	Design for testability	WE Ch. 7	
10010	8-Apr	In-class design reviews		Leaf cells complete
10011	10-Apr	In-class design reviews		
10100	15-Apr	Power and clock distribution	WE 4.7-4.8	
10101	17-Apr	Skew-tolerant circuit design	Harris: STCD	Final Project due
10110	22-Apr	Asynchronous design		
10111	24-Apr	Low power design		PS 5 due
11000	29-Apr	Yield, reliability, and scaling, and economics	WE 4.11-4.13	
11001	3-May	A History of Intel Microprocessor Chips		PS 6 due

Note: Final project presentations will take place during presentation days May 6-8