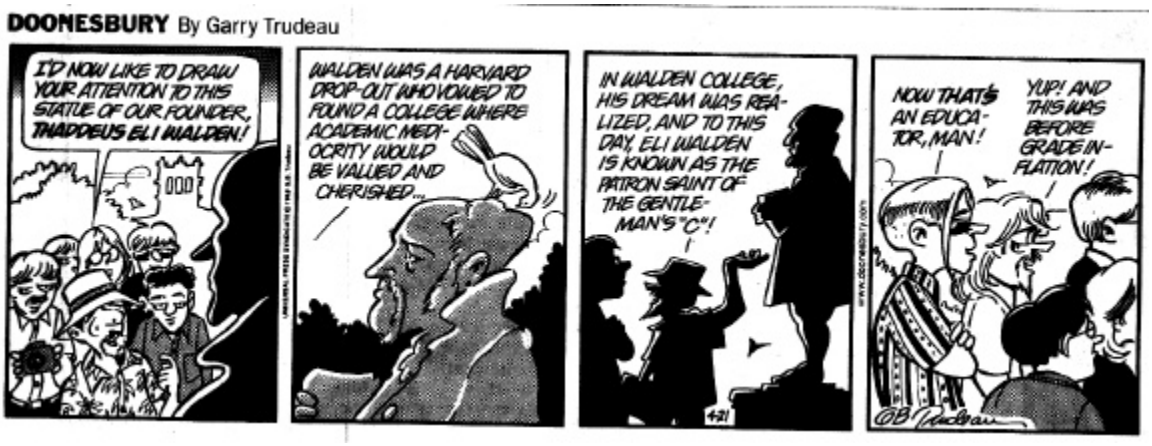
Harris

Introduction to CMOS VLSI Design (E158)

Problem Set 2



1. Compound Gate Design

A carry lookahead adder uses the following AOAO logic gate to compute the carry out of a 3-bit group from the generate and propagate signals for each bit in the group:

Cout = G2+P2• (G1+P1•G0)

a) Sketch a transistor-level schematic for a single compound gate that computes the complement of Cout.
b) Sketch a stick diagram for your gate from part (a).
c) Estimate the width and height of your cell based on your stick diagram.

2. Time

Please indicate how many hours you spent on this problem set. This will not affect your grade, but will be helpful for calibrating the workload for the future.