Harris

Introduction to CMOS VLSI Design (E158)

Syllabus

Spring 2001

Teaching Staff

Professor: David Harris Parsons 2374 x73623 David_Harris@hmc.edu

Schedule

Lecture: MW 1:15-2:30
Office Hours: TBD

I am in my office more often than not, so feel free to stop by even if I do not have official office hours.

Texts

Weste & Eshraghian, *Principles of CMOS VLIS Design*, 2nd Edition, Addison-Wesley, 1993.
Patterson & Hennessy, *Computer Organization & Design*, 2nd Edition Morgan Kaufmann 1998.
Sutherland, Sproull, and Harris, *Logical Effort*, Morgan Kaufmann, 1999.
Harris, *Skew-Tolerant Circuit Design*, Morgan Kaufmann, 2001.

Principles of CMOS VLSI Design is the required text. You will need it for weekly readings and for reference on problem sets and labs. It is somewhat dated, but still has the best coverage of the fundamentals of any book in the field. *Computer Organization and Design* is the E85 textbook. You will be building a MIPS processor in this class following the design in the book, so it is assumed that you have access to the book and are familiar with the MIPS assembly language from Chapter 3, ALU design from Chapter 4, and the multicycle processor microarchitecture from Chapter 5, as well as combinational logic design and finite state machine design from Appendix B. Consider this knowledge a prerequisite to the class and get yourself up to speed if you feel rusty. *Logical Effort* and *Skew-Tolerant Circuit Design* are two of my books and are recommended reading if you are considering graduate school or professional practice in the field of chip design.

Electronic Communication

Class web page: http://www3.hmc.edu/~harris/class/e158
Class email list: eng-158-l

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

subscribe eng-158-l

You also will need a computer account in the Engineering Design Center to complete your labs. If you do not have one or have forgotten your password, see a system administrator.

Grading

Labs:	30% (5% each for labs 1-4, 10% for lab 5)
Final Project:	30%
Problem Sets:	15%
Final Exam:	25%

The emphasis of this class is hands-on chip design. During the first six weeks, you will complete a series of labs to build your own MIPS microprocessor. Along the way, you will master a variety of CAD tools and design techniques. Based on this experience, you and a partner will propose and carry out a final project of your choosing. If we are fortunate, we may be able to fabricate some of the final projects.

As you will discover, hands-on design is extraordinarily time-intensive. It is impossible for you to apply all the knowledge you gain from this class to an actual design, so a series of problem sets will give you an opportunity to master these concepts. The final exam will reflect both the material from the problem sets and labs.

Labs and problem sets are due by the end of class and will not be graded if submitted late because solutions will be given out. However, the labs build toward assembly of the entire processor in Lab 6, so it is important not to fall behind. Your lowest lab and homework score will be dropped before the average is calculated. You are welcome to discuss labs and problem sets with other students or with the instructor **after** you have made an effort by yourself. However, you must turn in your own work, not work identical to that of another student. Be sure to credit at the top of your assignment anyone with whom you discussed ideas. **It is an honor code violation to simply copy someone else's work.**

In the event of a power failure of greater than 15 minutes on the day before an assignment is due, an extension is automatically granted until 5pm on the day after the assignment would ordinarily be due. No further extensions are granted even if a second power failure occurs.

Tentative Schedule

The attached schedule is a tentative plan that may change during the semester. The deadlines, however, are fixed unless otherwise notified; *do not assume* that they will change just because the lecture schedule changes.

The schedule lists recommended readings with each lecture.