The Zailinx FPGA Final Report

E158 Final Project
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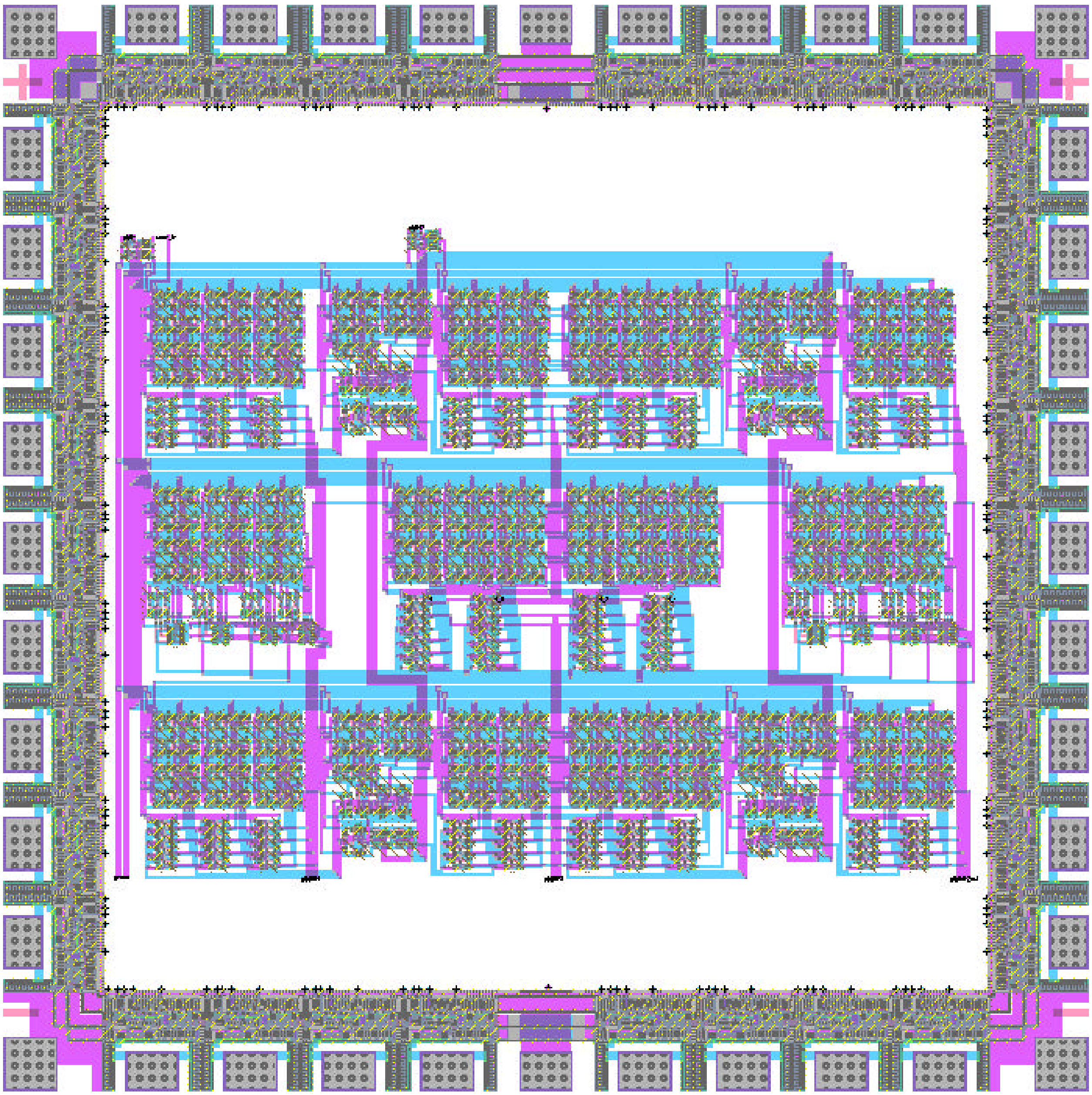
11 April, 2001



Functional Overview

The Zailinx FPGA is a scalable field programmable gate array design that can simulate simple combinational logical functions and sequential logic. It achieves this functionality though the four combinational logic blocks (CLB), each of which contains a two-input look-up table (LUT) and a flip-flop. Connecting the CLBs together is a network of configurable switches joined by three rows and one column of four-wire bus. In addition, there are connection blocks that allows each of the CLB I/Os to be connected to any of the adjacent vertical interconnect.

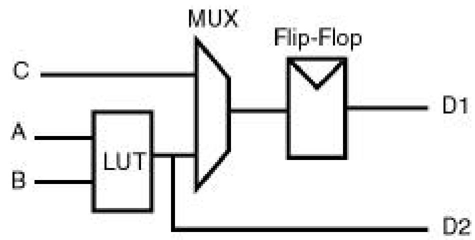


Figure 1 - The CLB schematics

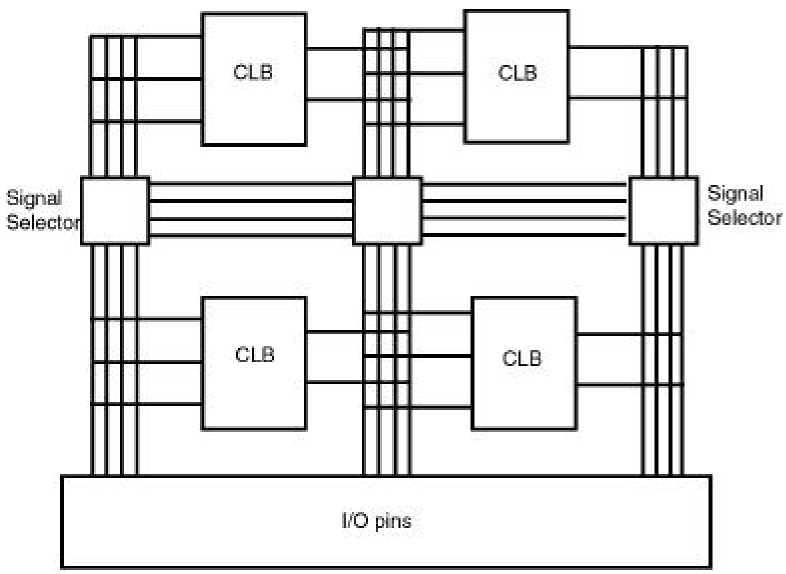
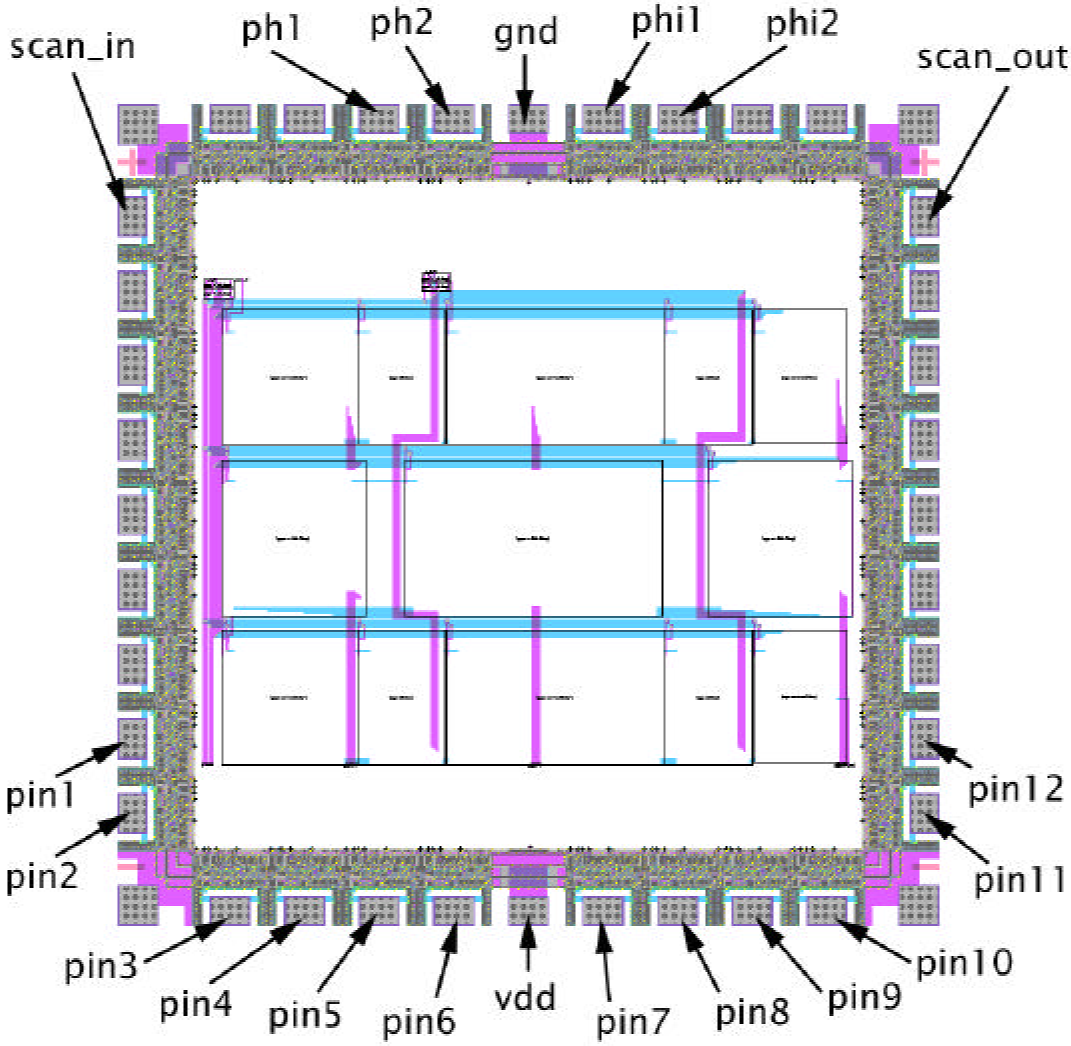


Figure 2 - The interconnections between CLBs

Configuration of the chip can be achieved by sending serial data through a shift-register, called a scan chain. This approach only requires three pins dedicated to configuration: a two-phase clock that drives the shift-register; and the valid configuration data. At every clock period, each flip-flop of the chain passes configuration data down the chain. Configuration is complete when the shift-register contains a valid and correct configuration data. At the end of the scan chain, the output of the final flip-flop is attached to an output pin for ensuring the configuration scan chain is working properly. Each configuration data bit will be responsible in controlling arrays of multiplexors and transmission gates that determine how signals are connected between the CLBs and the input/output pins, as well as inputs for the look-up table within each CLB, for the FPGA to achieve the desired functionality. Each user-interfacing pin can be connected to either a CLB input or output, thereby increasing the flexibility of the system.

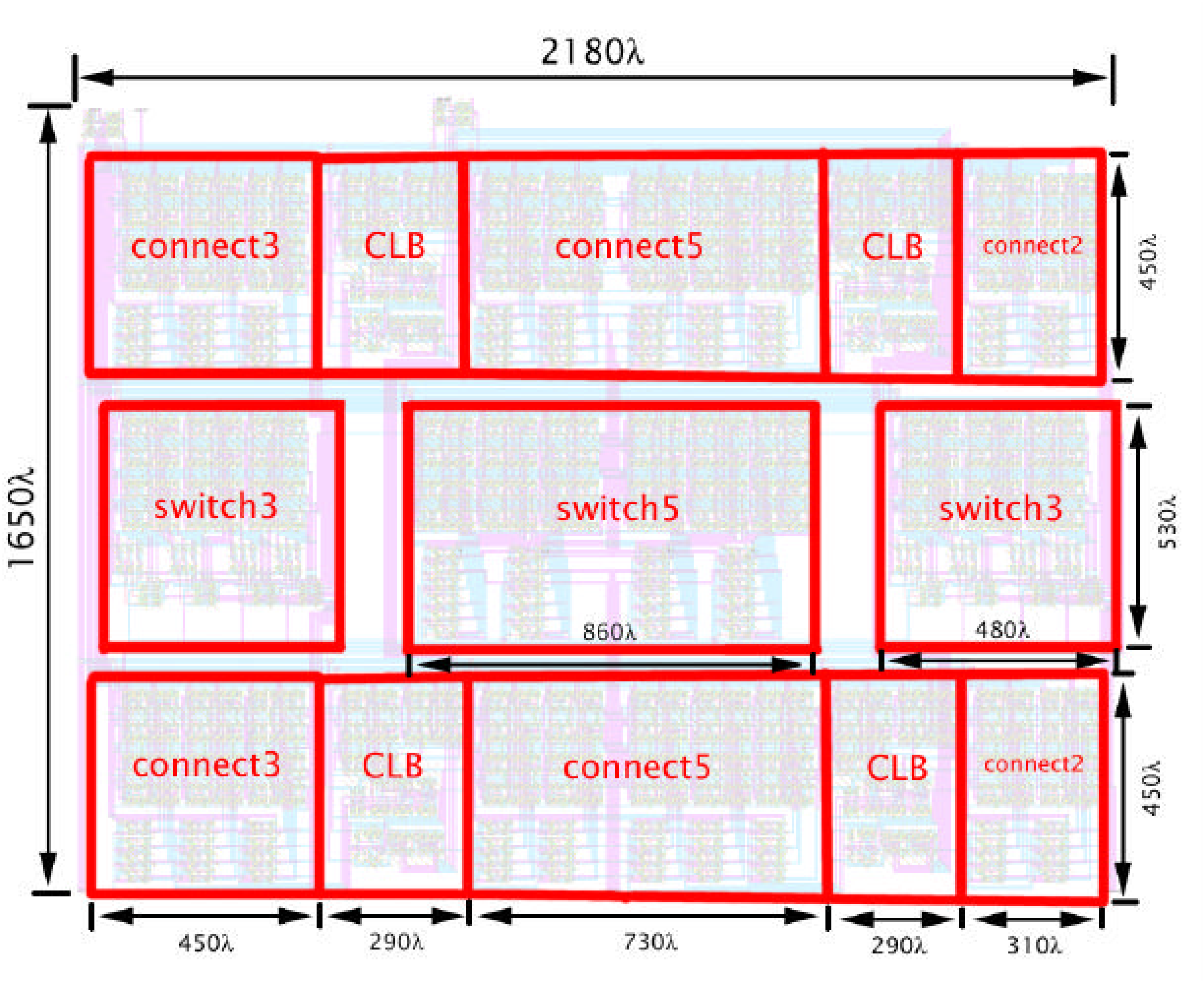
The scan chain is embedded within each CLB, connect logic and switching logic. Each facet has its own segment of the chain that are connected to neighbouring facet blocks to produce one complete scan chain. This allows the design to be scalable by attaching extra connect, switching logics and clbs if given extra chip space, without redesigning any of the blocks.

Chip Pinout



Pin(s)	Pin Type	Pin Description
vdd	Power	Provides power to the chip
gnd	Ground	Provides a relative ground to the chip
ph1 & ph2	Clock	Two-phase clock that triggers all the flip-flops in the scan chain. Needed for FPGA configuration.
scan_in	Input	Input to the scan chain. This is where configuration data is fed into the FPGA when working in conjunction with ph1 and ph2.
scan_out	Output	Output from the scan chain, useful for debugging.
phi1 & phi2	Clock	Two-phase clock input that acts as the global clock of the flip-flops that resides in each CLB.
pin1 - 12	Bidirectional	The 12 I/O pins of the FPGA. These are configured either as input or output depending on the desired function and configuration of the FPGA.

Chip Floorplan



Facet	Estimated Size	Actual Size	Design Time
Overall Footprint	2100λ x 1600λ	2180λ x 1650λ	32 hrs (est.)
clb	860λ x 530λ	290λ x 450λ	3 hrs
connect2	80λ x 80λ	310λ x 450λ	2 hrs
connect3	80λ x 80λ	450λ x 450λ	10 hrs
connect5	80λ x 160λ	730λ x 450λ	2 hrs
switch3	40λ x 80λ	480λ x 530λ	8 hrs
switch5	60λ x 80λ	860λ x 530λ	2 hrs

Note: The estimated size of each facet was based on the initial design where the scan chain is not integrated into each clb, connect logic and switching logic. Therefore the estimated and actual sizes differ drastically. Despite the change in design, the actual overall footprint matches the estimate well.

Simulation

I was unable to perform simulations due to personnel reasons.

Verification Results

Facet	DRC	ECC	NCC
inv	**P**	**P**	**P**
inv4x	**P**	**P**	**P**
tri	**P**	**P**	**P**
mux2	**P**	**P**	**P**
mux4	**P**	**P**	**P**
latch	**P**	**P**	**P**
flop	**P**	**P**	**P**
clb	**P**	**P**	**P**
connect2	**P**	**P**	**P**
connect3	**P**	**P**	**P**
connect5	**P**	**P**	**P**
switch3	**P**	**P**	**P**
switch5	**P**	**P**	**P**
FPGA	**P**	**P**	**P**

Test Plan

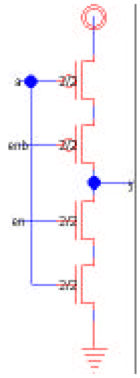
1. **Scan Chain Test**: Put a constant 'high' signal on the scan_in pin and then clock ph1 and ph2 appropriately. After 148 cycles, if the scan chain is functioning correctly the scan_out pin should become 'high'. To test this further, input a known test vector in to the scan_in pin (say, alternating 1's and 0's) and see if the configuration data is pushed through the chain correctly.
2. **Swiching Logic Test**: This test connects pin 12 to pin 8 using the switching logic within the FPGA. The right-most *switch3* block should have configuration data '100 000 000 000' in order to connect *v4b* to *h4*, the *switch5* block should have configuration data '000100 000000 000000 000000' to connect *v4b* to *h4b*. Therefore the overall configuration data stream is 50 zeros followed by a 1, and then 14 zeros, a 1, and finally 82 zeros. Once the FPGA is configured, change the input to pin 12 and see if the voltage on pin 8 follows and vice versa.
3. **CLB Test**: This test involves configuring the bottom left CLB to test the look-up table and its flip-flop. The CLB configuration data is '10111' to configure the LUT as a NAND and the input to the flip-flop to use *in3*. The connect2 block to the right of this CLB should be configured with '1000 0001' to connect the output of the CLB's flip-flop to pin 12, and the output of the LUT to pin 9. The connect5 block to the right of the CLB should be configured with '100010 000001 000000 000000' to connect the two inputs of the LUT to pins 7 and 8, and the input to the CLB's flip-flop to pin 5. Therefore, the overall configuration data should be '1000 0001 10111 1000 1000 0001 0000 0000' followed by 115 zeros. Once configuration is complete, test the CLB functionalities by ensuring that the output pin 9 is the NAND of pins 7 and 8. Also, test the CLB's flip-flop by clocking it though the phi1 and phi2 pins and seeing the data value of pin 5 passed to pin 12 correctly every clock cycle.

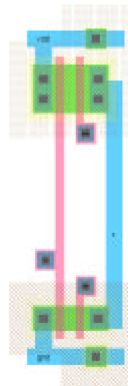
If the chip passes all of the above tests, then the chip should be functioning as the design intends it.

Schematics and Layout

Tri

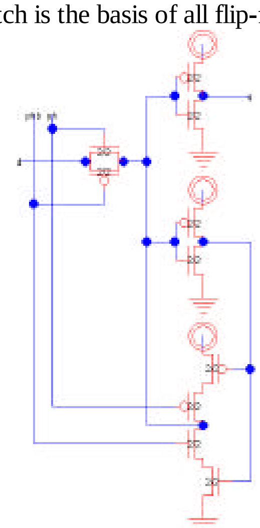
This is the tri-state used to build the muxes on the chip.

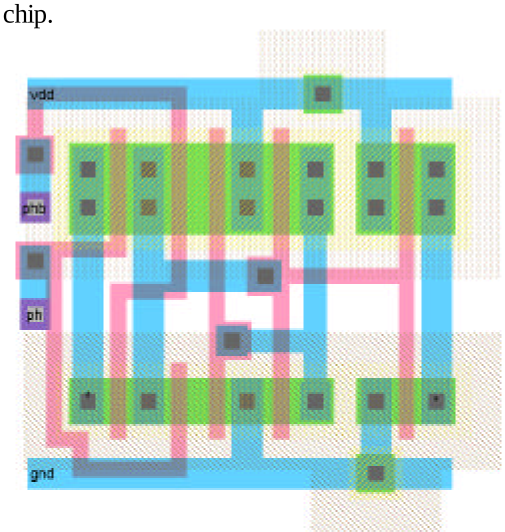




Latch

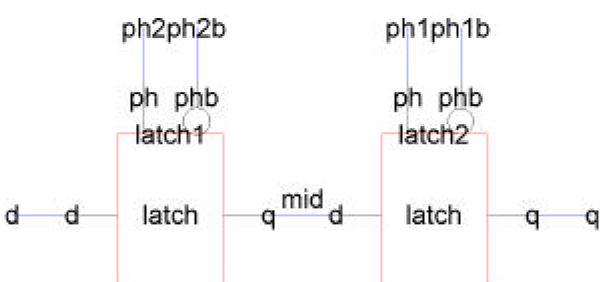
This latch is the basis of all flip-flops on the chip.

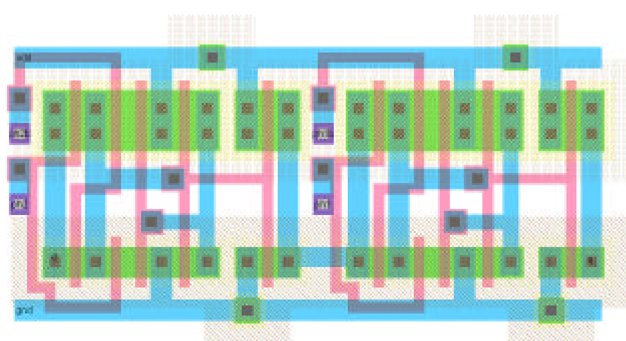




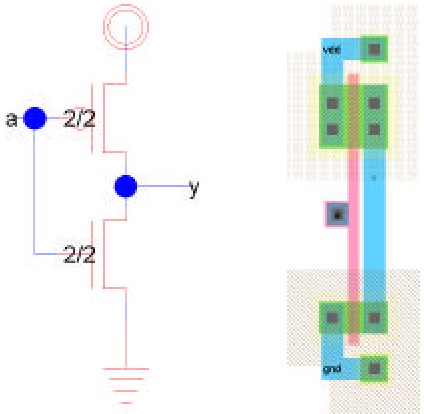
Flop

The flip-flop is based off the std- mudd design except the height has been shrunk to 50 λ (there are 138 flip-flops on the chip and space is limited). Also, the

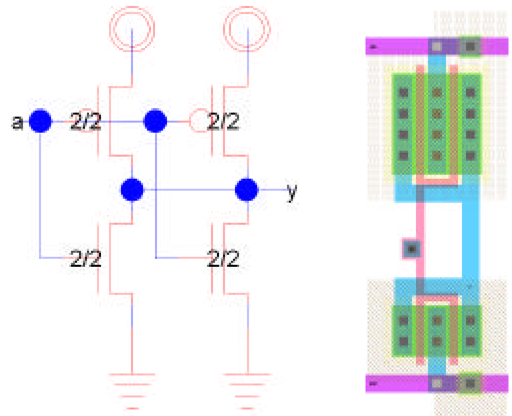




inv

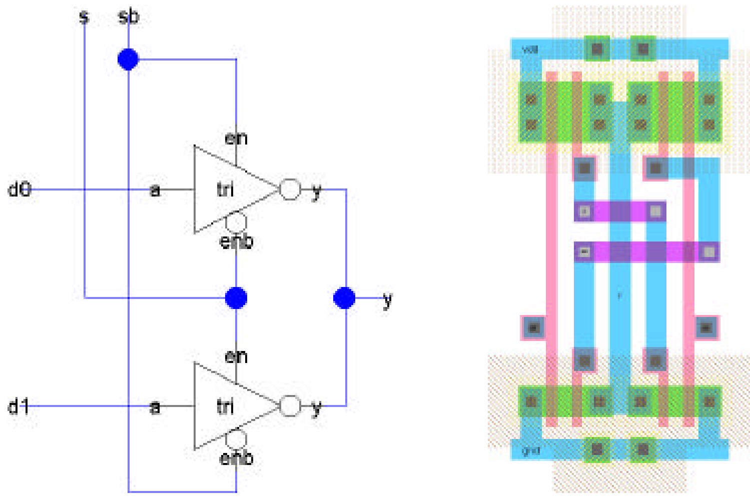


inv4x



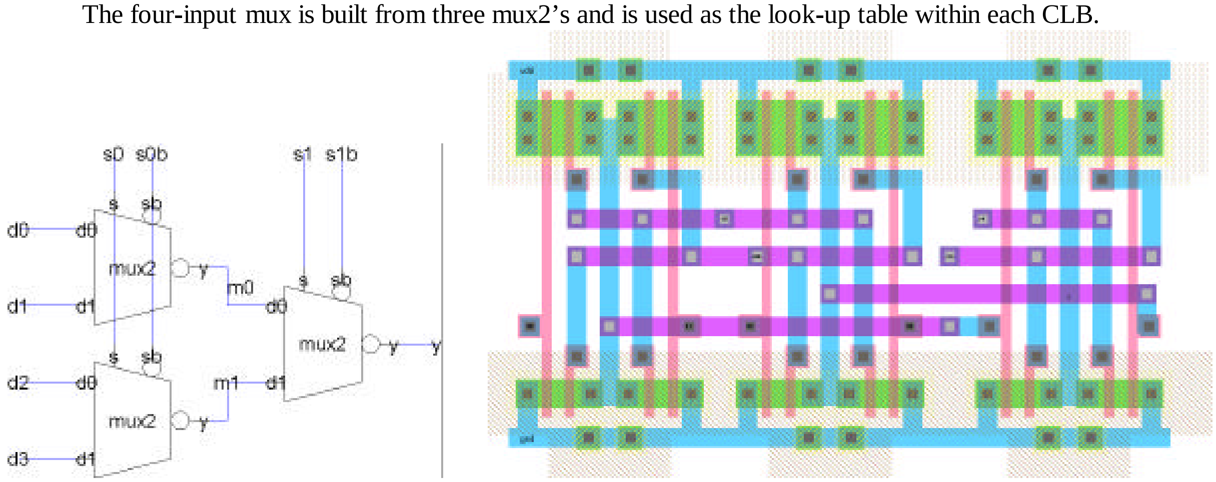
mux2

The two-input mux is based off the std-mudd mux2, and used within each CLB to select the signal going to the CLB's flip-flop.



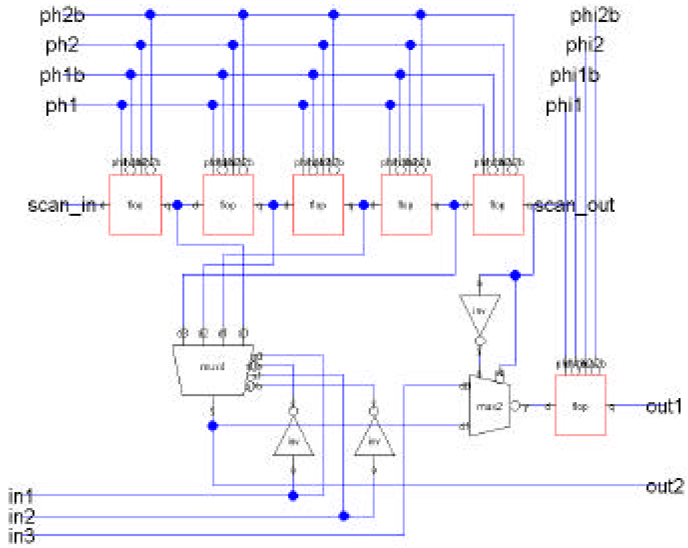
mux4

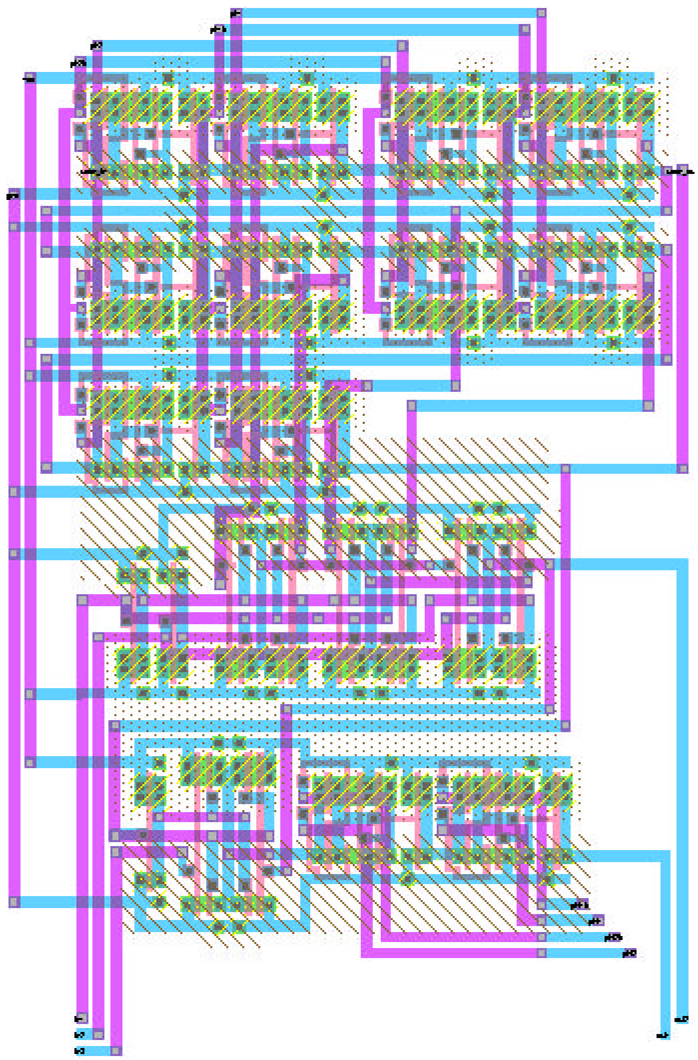
The four-input mux is built from three mux2's and is used as the look-up table within each CLB.



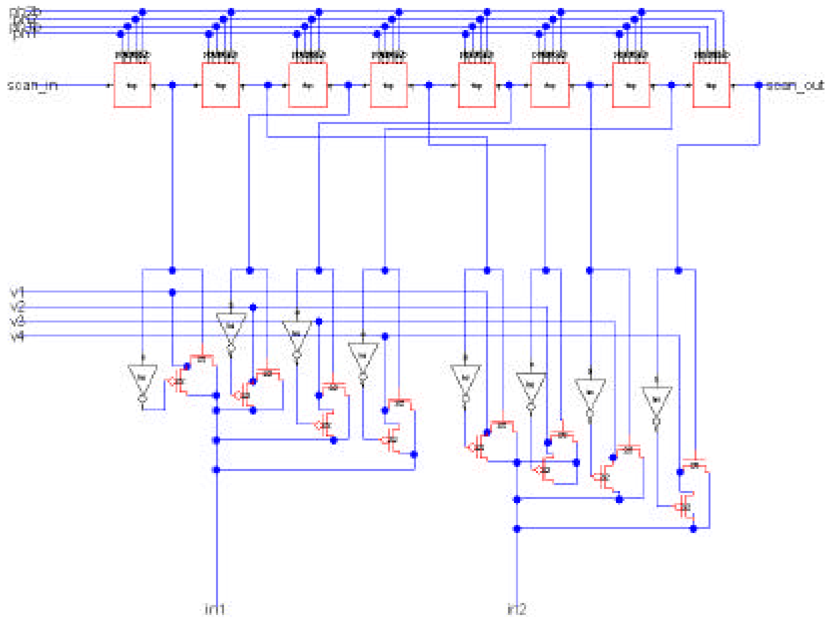
CLB

The CLB contains five configuration flip-flops, four of the configuration bits are used as data input to the look-up table, while the last configuration bit decides whether the input of the CLB's flip-flop is connected to the output of the LUT or an input pin. Inverters are placed as necessary to provide the complementary select signals that the muxes need.





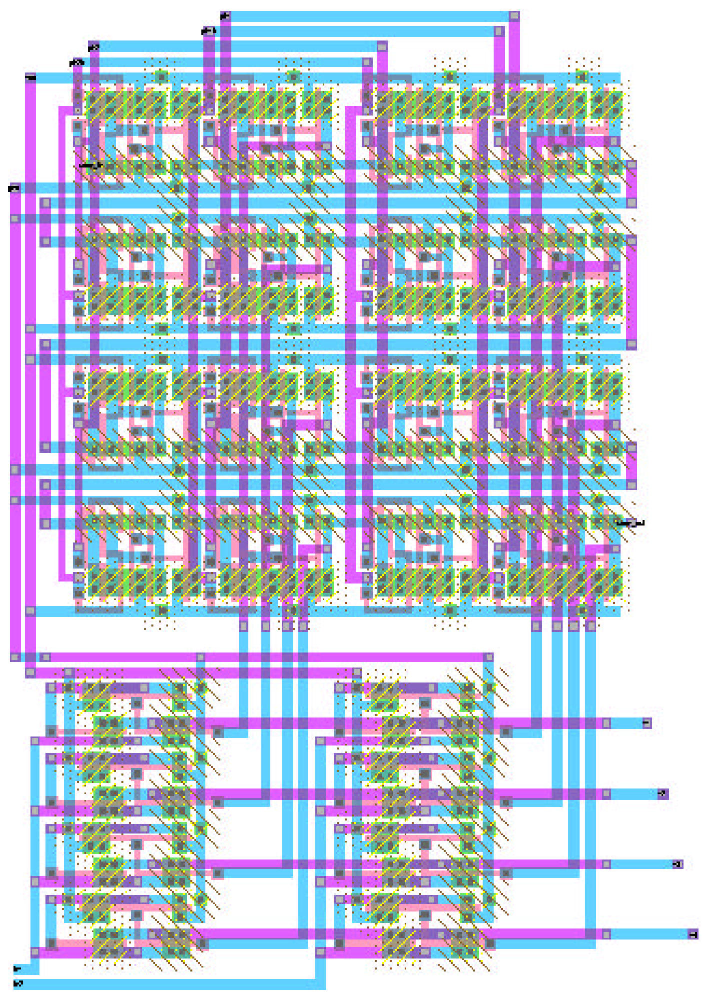
Connect2



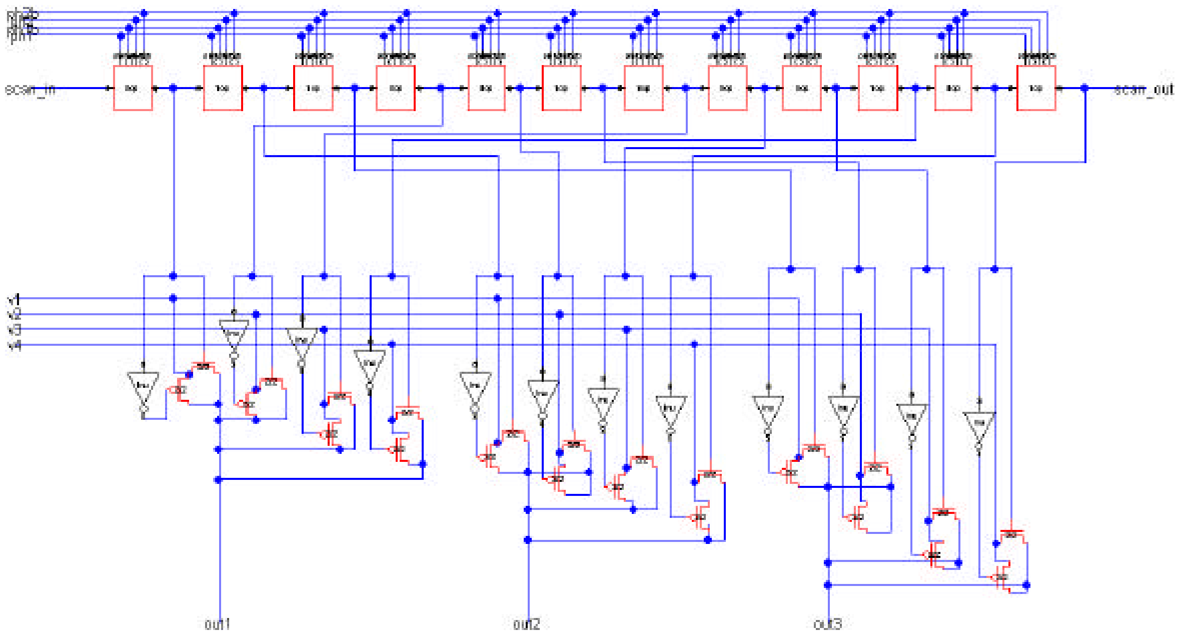
The *connect2* facet determines how the two outputs of a CLB is connected to the vertical interconnects. Each of the CLB output is connected to four transmission gates, allowing each CLB output to be connected to any of the interconnects.

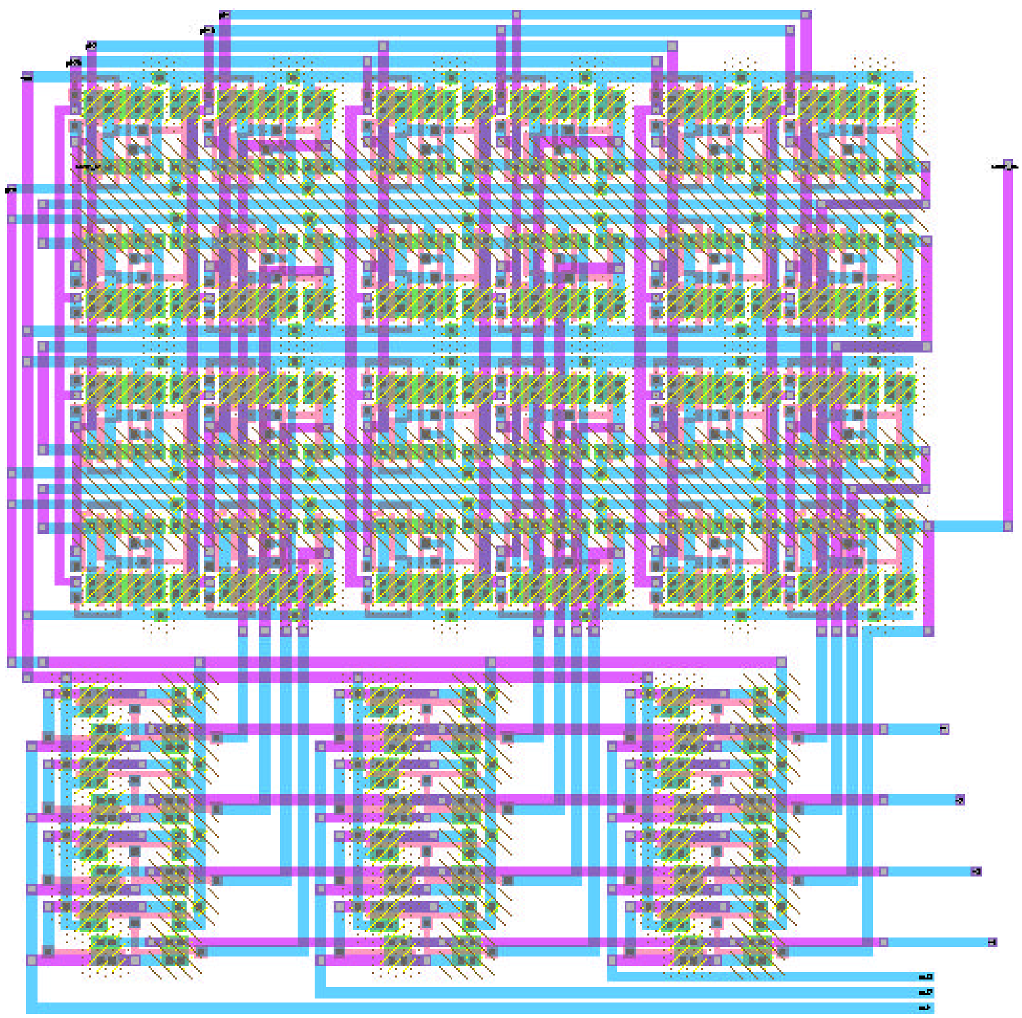
The *connect3* facet is an extension of the *connect2* facet. It has the same functionality as *connect2* except that it determines how the three inputs of the CLB are connected.

The *connect5* facet is basically a *connect2* block and a *connect3* block merged together. It is positioned between two CLBs to handle the outputs from the left CLB and the inputs to the right CLB.

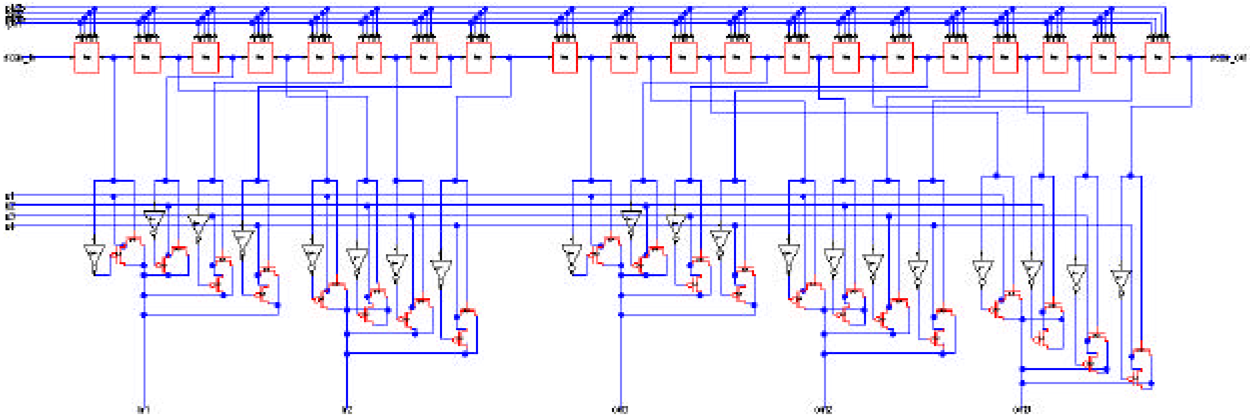


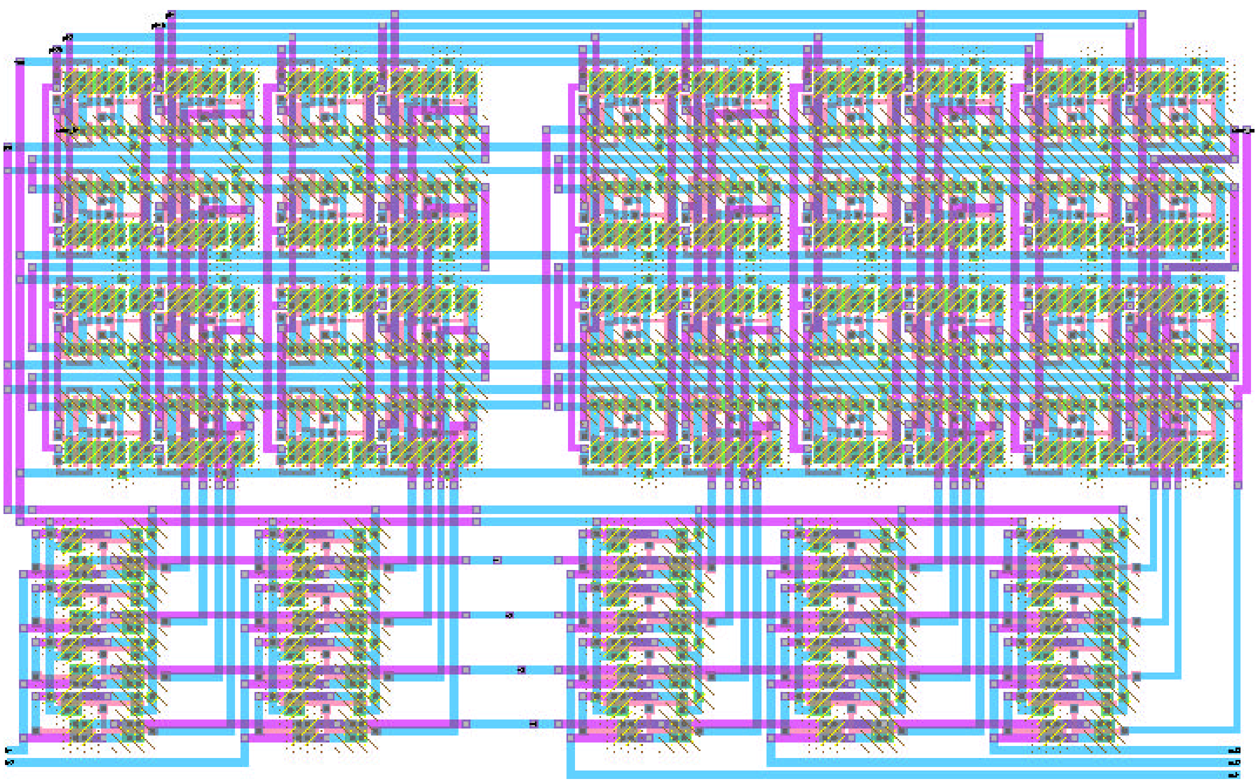
Connect3



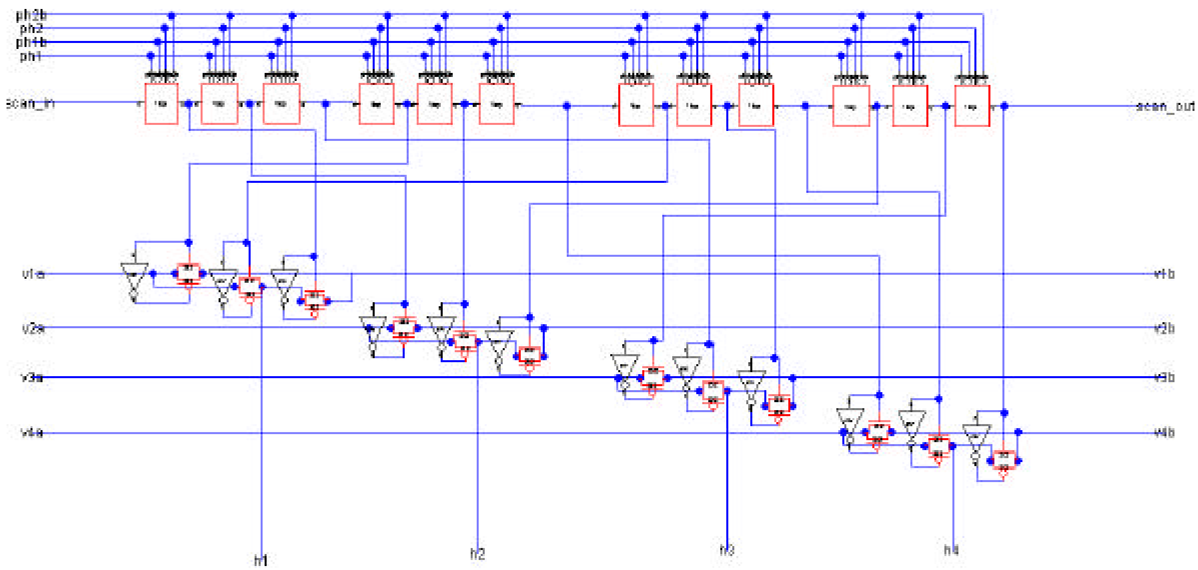


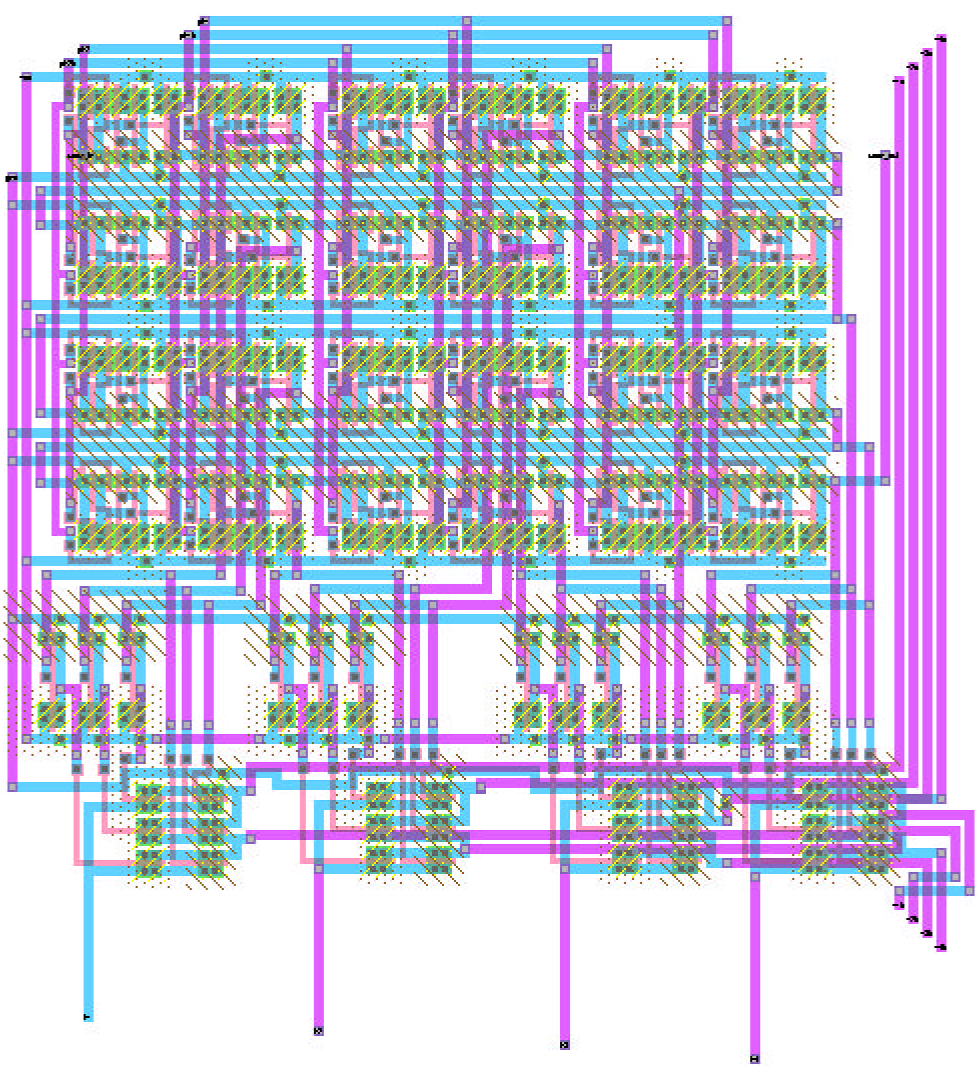
Connect5



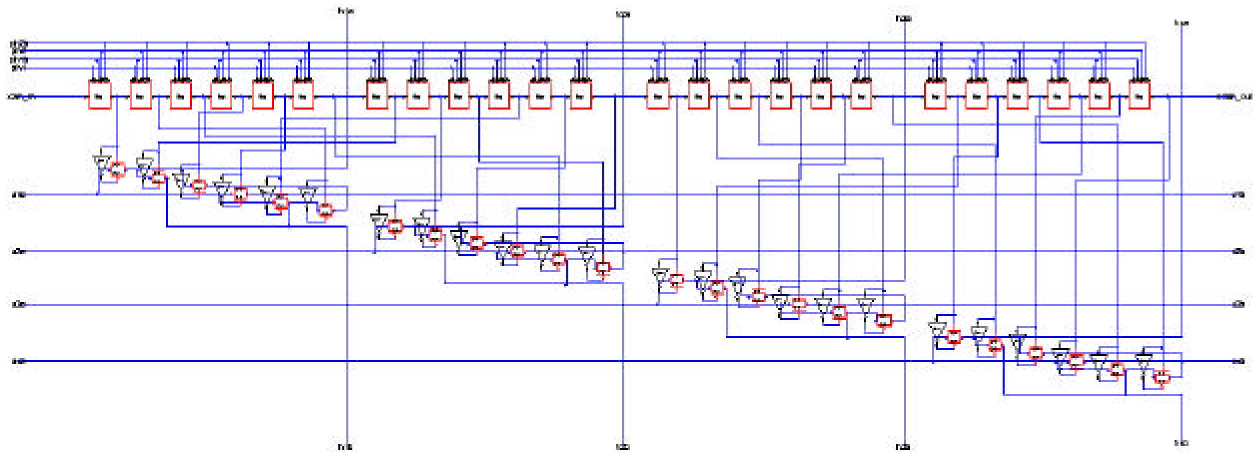


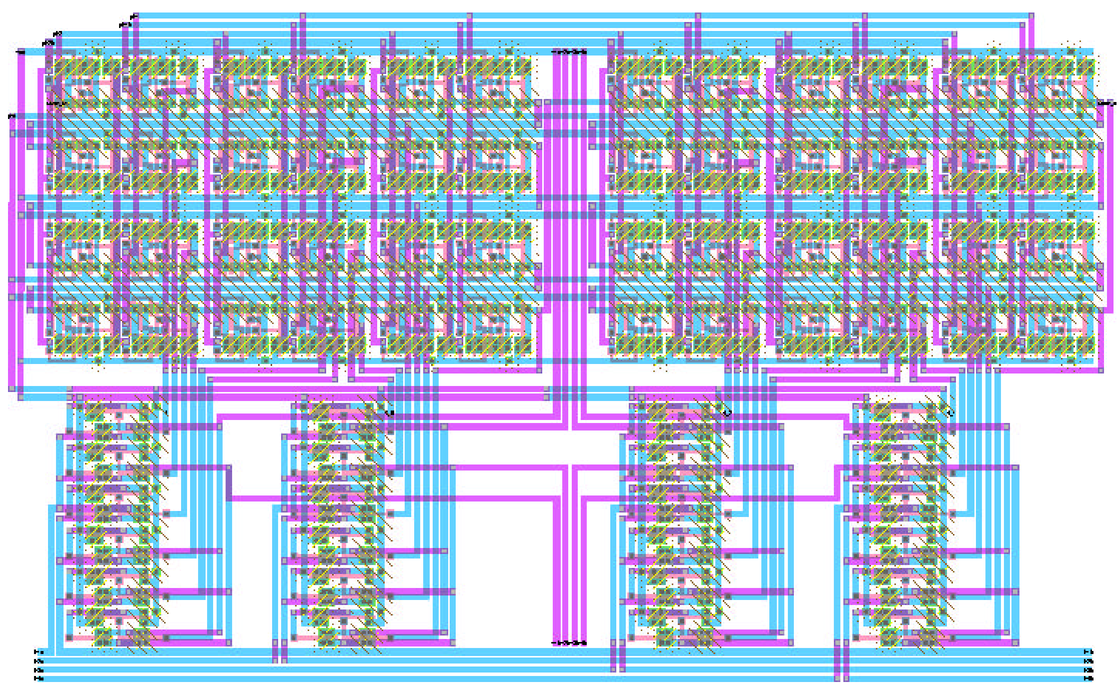
Switch3


ph2b
ph2
ph1b
ph1
scan_in
scan_out
v1a
v2a
v3a
v4a
v1b
v2b
v3b
v4b
h1
h2
h3
h4

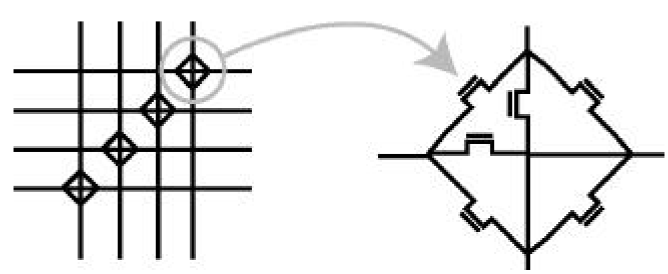


Switch5





switch3 and switch5 allow the vertical and horizontal interconnects to be connected in a variety of manner. The basic set-up are six transmission gates mediating one vertical and one horizontal interconnect signals shown on the right. As before, its corresponding portion of the scan chain is attached to it.



FPGA

The top-level design involves simply connecting each of the blocks to its neighbours, generating complementary clock signals and distributing the scan chain clocks to all facets. The global clocks (and their complementaries) of the CLBs' flip-flops are also connected together. In the top level design, the different fragments of the scan chain are connected to produce the entire scan chain.