Harris

Introduction to CMOS VLSI Design (E158)

Final Project

1. Overview

The E158 Final Project is a chance for you to apply your new skills in VLSI design to a moderate sized problem of your choosing as part of a two-person team. You should begin thinking about a project and teammate right away. Your project has the following milestones:

2/28:	Project Proposal Due
3/7:	Floorplan Complete
3/21:	Schematics Checkoff
4/2:	Leaf Cells Complete
4/11:	Final Project Checkoff, Report Due
4/16-4/18:	Project Presentations

2. Project Suggestions

Be creative when selecting your project. Your project should be bigger than a 1-week lab assignment, but small enough to be doable. If in doubt, err on the side of smaller; you will receive a much better grade for a simple project that is completed and convincingly verified than a large project that is incomplete.

Your project should fit on a 2.2 x 2.2 mm 40-pin MOSIS "TinyChip" fabricated in a 1.5 μm process. That means your project must not exceed 2750 x 2570 λ including I/O pads. Therefore, the core of your project must fit in a 2200 x 2200 λ box and have no more than 40 pins. Six pins are dedicated to VDD/GND, so only 34 are available as I/Os. Exceptions may be made for project proposals that need to exceed this area or pin count but are simple enough to be feasible in the time allotted; such projects will not be placed in a pad frame. Unless negotiated in the proposal, there will be a grade penalty for exceeding the area available.

Your project should include the layout of at least two new leaf cells and some cells organized as a datapath or array; do not just synthesize a bunch of Verilog and feed it to the Silicon Compiler. Examples of suitable projects are listed below, but do not let the list limit your imagination!

- Carry lookahead or Tree Adder
- Array Multiplier
- SRT Divider
- Alarm Clock
- MIPS processor with new instructions
- Tiny FPGA
- Area-efficient decoder and register file for E158 labs
- Digital Signal Processing unit
- Encryption or Decryption circuitry
- Clinic-related circuits
- Games (tic-tac-toe, checkers, etc.)
- Cache memory
- CORDIC function generator
- ROM or PLA

CAD projects involving improvements to Electric may also be acceptable. If you are considering such a project, discuss it with the instructor before submitting your proposal.

3. Design Budgeting

One of the challenges of chip design is to learn to budget your time and area. Experience is crucial to doing this well. One of the elements of the project will be to track this data so that you can learn to budget in the future.

Early in your project, you will submit a floorplan with area estimates. At the conclusion of the project, you will submit a comparison between the initial estimates and the actual results, along with an explanation of discrepancies.

Even more importantly, track the time you spend on the project. Keep a notebook and update it each day you work on the project. Note how much time you spent on each facet. Include the time spent designing the schematic, icon, and layout as well as time spent for simulation, DRC, ERC, and NCC.

4. IC Fabrication

Harvey Mudd has received funding from the MOSIS Educational Program to fabricate up to 6 TinyChip projects. If your chip is fabricated, you will receive 5 packaged parts in the fall. Priority for fabrication will be given to teams on the following basis:

1. Layout fits on a 40-pin MOSIS Tiny Chip and is wired to the pad frame provided.
2. Layout passes all DRC, ERC, and NCC tests and simulates successfully
3. At least one teammate is on campus in the fall and is committed to testing the chip.
4. Among teams meeting the above qualifications, the teams receiving the highest grades will have priority to fabricate.

5. Deliverables

Your team is responsible for the following deliverables on the dates described above:

Project Proposal

A 2-page proposal describing what you plan to build. It must be specific enough that the instructor can determine when you demonstrate your project that it meets the specs of the proposal. The proposal should also include a table listing all the inputs, outputs, and bidirectional pins on the chip

Floorplan Complete

A brief report describing the facets used in the design and the chip floorplan. It should list every facet that will be used in the design and the estimated areas of each facet. State the number of unique leaf cells that must be drawn. The floorplan should show how the overall chip will be partitioned into major units and how the units will be physically arranged. All of the interconnections between these units should also be specified.

Schematic Checkoff

Schedule a checkoff with the instructor to demonstrate that the schematics are complete and simulate successfully at the top level. Be sure that your simulations demonstrate complete operation of the functionality specified in the proposal.

Leaf Cells Complete

A brief report listing each leaf cell in the design. With each cell, compare the actual cell area to the estimate from the floorplan.

Final Project Checkoff

Schedule a checkoff with the instructor to demonstrate that the project is complete. Show a clean, complete layout in a pad frame. Show that the layout passes DRC, ERC, and NCC. Show that either the schematic or layout simulates and satisfies the specifications of the project proposal.

Final Report

The final reports should include the following items:

- Cover page with color chip layout
- Functional overview
- Chip pinout
- Chip floorplan

- Area and design time data
- Simulation results
- Verification results: DRC, ERC, NCC
- Test plan
- Complete schematics
- Complete Verilog (if applicable)
- Complete layout

Your final report should convince the reader that your design would function and meet specifications if fabricated. It should also provide all the information another engineer would need to know to test your chip after fabrication. Turn in a PDF version of the report to post on the class web page and a hard copy to grade.

Project Presentation

You will give a 10-minute in-class presentation of your chip. Your presentation should explain your design and your results to your classmates. It should include a functional overview, the chip pinout and floor plan, simulation and verification results, and a top-level chip layout. The presentation should be in PowerPoint or PDF format for projection in class.

6. Grading

Your project will be graded as follows:

Proposal	10%
Floorplan	5%
Schematic Checkoff	10%
Leaf Cells Complete	5%
Final Checkoff	25%
Final Report	25%
Presentation	20%

If you feel there has been inequity between the work you and your teammate deliver, contact the instructor.

As we all know, Electric is not a perfect tool yet. Keep regular backups of your project should Electric corrupt your library (very rare, but potentially very bad). Should you encounter a serious bug that prevents you from verifying part of your project, seek a workaround. If you cannot find a workaround, contact the instructor; your grade will not be penalized if the design should be possible to verify with a better tool but hits a limitation in Electric.