Serial Protocol Decoding on the RIGOL MSO1104z
E155
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Configuring the Decoder for SPI Decoding

1. Connect the logic analyzer ribbon cable and Active Logic Head (RPL 1116). This peripheral is not hot-swappable, so make sure the scope is off before you connect it. Note that unlike the BNC probes, each grabber only makes one connection and so 2 grabbers must be used for each DATA/GND pair. (i.e., do not connect a signal wire and ground wire to the two grabber terminals. You will be shorting your signal to ground!)
2. Press "MATH > Decode1" and select your protocol from the "Decoder" menu option. For this example, we will configure the SPI decoder.
3. Configure the menu items to select the proper data lines for CLK, MISO, and MOSI. In this example CLK is on D1, MISO is on D3, and MOSI is on D2.
4. To enable the decoder, toggle the "Decode" option to "ON".
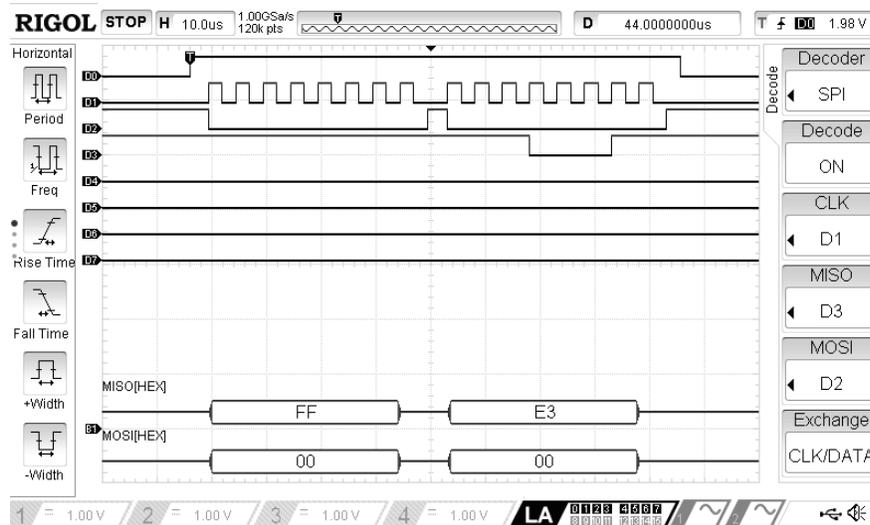
5. If you scroll down the side menu by pressing the down key to the right side of the screen you can configure other options. In general, using the chip select mode will be the most successful way to get the decoder to work properly. To enable this mode select "CS" in the "Mode" field and then select the appropriate data line (e.g., D0) in the "CS" field. You will also need to configure a few other options such as whether the chip select is active high or low and whether the chip select leading edge is a rising or falling edge.
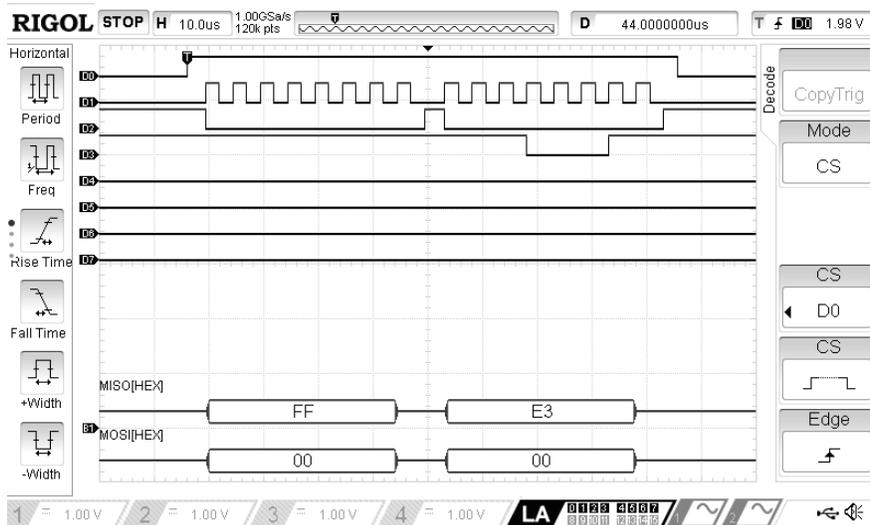
6. Scroll down the side menu to the third menu page to configure other parameters such as the polarity, data packet width, bit order, and format.
   a. Polarity: Whether a logical one is a low or high digital signal.
   b. Width: The length of each data packet in bits.
   c. Order: Whether the data packets should be interpreted as most significant or least significant bit first.
   d. Format: The way to interpret the serial data. Options are hexadecimal (HEX), decimal (DEC), binary (BIN), ASCII (ASC), or LINE. The LINE mode displays the raw series of binary data without any modification. If the bit order is selected as MSB, then LINE and BIN are equivalent.
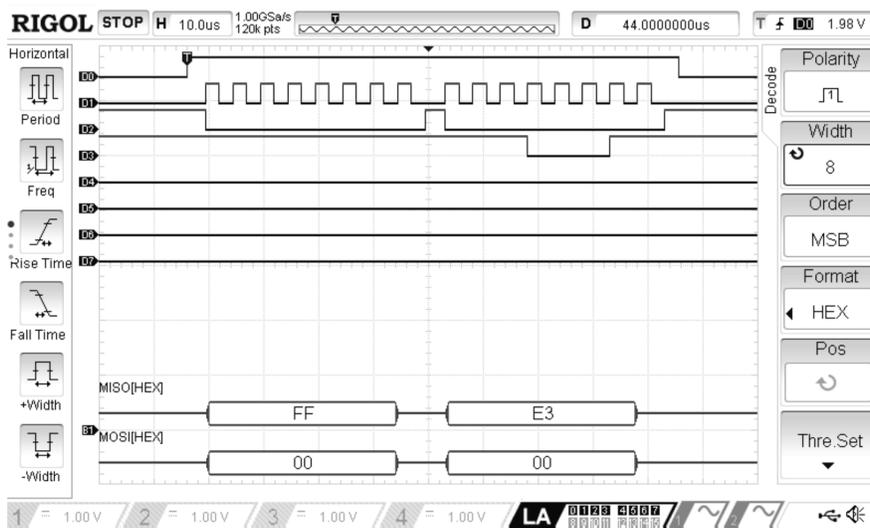
Troubleshooting

If your logic analyzer traces are showing glitches, you may need to recalibrate the probes. To do this you can find the "Probe-Cal" option by selecting the "LA" channel and then scrolling down one menu on the right side of the screen. Then you must disconnect everything from the wires attached to the input of the RPL1116 Active Logic Head and run the calibration. If this calibration procedure fails, you may need to reset the scope to default settings and try again (by pressing Storage > Default).