Digital Alarm Clock

E157 Final Project Final Report

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Abstract:

Digital alarm clocks typically use 7-segment LED's as its display, and a count-up scheme for changing the clock time and alarm times. With the availability of a twelve key keypad and LCD screen, a simple alarm clock can look much sharper, and work much better. Such a clock is constructed by combining the E157 FPGA board with the HC11 to control and generate the keypad inputs and LCD display outputs. The FPGA and the on board clock oscillator will generate accurate timing signals and debounce keypad inputs, while the HC11 will store the time value, handle alarm clock functions, and generate the control signals to the LCD. The audible alarm will simply be a square wave signal generated by the FPGA amplified by a set of external computer speakers.

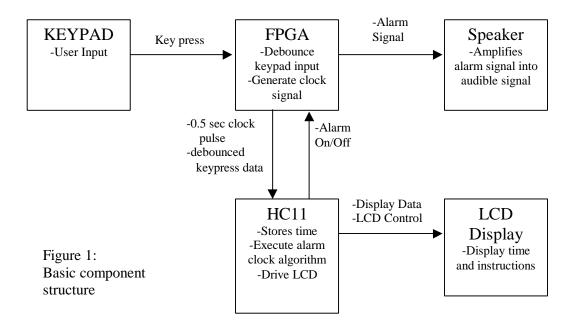
Introduction

The motivations behind the choice of the alarm clock as a final project are the following: its utilization of both the FPGA and the HC11, its use of an LCD display, and, finally, its advantages over a conventional digital alarm clock.

The final project requirements are met by the tasks required of both components. The HC11's memory capabilities is used to store and increment time information, while its capability to perform more complex sequential tasks streams the functions such as changing into an editing mode for time editing, etc. The FPGA board uses an external oscillator that generates accurate clock speeds. This fact makes the FPGA an ideal choice for generating accurate timing signals. The FPGA also handles the debouncing of the keypad input since the procedure is best handled by permanent logic. In short, both components are important counterparts of each other for the alarm clock.

In addition to being a suggested component for a final project, the LCD screen is a great component for the purposes of displaying numbers and characters. The LCD screen's ability to display multiple characters allows for a friendlier menu-type display, replacing the various primitive methods of entering data into alarm clocks. Furthermore, the LCD display has on-board display memory and built-in character display functions (cursor position, pre-programmed characters, etc.). These features make the HC11 the single necessary component to drive the LCD display.

The LCD display digital alarm clock provides several advantages over regular alarm clocks. These advantages include having keypad input instead of the single-button up-counting input for commercial alarm clocks, and using an LCD screen for a sleeker display. The tasks performed by the individual components and the data they transmit are shown in Fig. 1.



New Hardware

PC Speakers:

The PC speaker set inside the Microprocessor lab includes a built in amplifier ideal for amplifying small amplitude signals, such as one generated by the FPGA in thisproject.

The built-in amplifier simplifies any project by avoiding extra amplifier circuitry,

especially when connection with the

speakers is a snap. For this project, the GND part of the speaker jack is wirewrapped with regular wire and connected to ground, while the tip of the speaker jack is connected to the signal source.

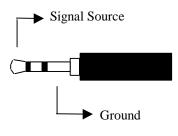


Figure 2: PC Speaker Connection

LCD Display:

The LCD display unit comes with a multitude of support circuitry on-board. The tasks of refreshing the LCD screen, temporary storing display information, character information, etc. are all handled by the memory and microcontrollers provided. The task of writing to the LCD becomes therefore a strict regime of following the manufacturer's directions.

Connections to the LCD display unit are made through the 14 pins on the board. The pin symbols are provided in both Appendix X and the spec sheets provided by the manufacturer.

The Vee pin provides power for the display unit itself. An exterior potentiometer is used to keep this voltage between the maxim of 5V (Vcc) and the low voltage. Adjusting this value effectively adjusts the contrast of the LCD display. If a potentiometer is not available, simply connecting the Vee pin to Vcc should suffice for testing purposes.

The RS pin is the "Register Select Signal." When driven high, the LCD unit will expect to receive data information. While low, the LCD unit will expect instruction input.

The R/W pin stands for Read or Write. When high, the LCD unit expects an instruction or data input into the system. When low, the LCD unit will actually send status information out to the controlling microcontroller. The write function was not utilized in this project.

The E pin is where the Enable signal is sent. This enable signal is the timing control for any information transfer in or out of the LCD unit. The enable cycle time

must be a minimum of 500 ns. As long as instruction transfer does not exceed 2MHz, information transfer should not be a problem. Like enable pins of other devices, pulling the enable pin high causes the LCD unit to read the data pins for information. The microcontroller should write data ports before pulling the enable pins high.

A intializing sequence must be followed for the LCD screen to start properly. The sequence provided by the manufacturers did not function properly or consistently, so an alternate sequence was used in its place.

Once initialized, the LCD unit is ready to receive data from the microcontroller. The LCD unit performs functions such as locating the cursor, flashing the cursor, etc. depending on the instruction it receives. When data is received instead of instructions, the LCD unit simply prints the character represented by the data at the cursor's current location.

Component Connections

The prototype alarm clock uses a solderless breadboard with basic 22wg wiring. Each component have pins which are numbered by manufacturer, or are noted in the diagrams below. The connections between pins are provided in appendix A.

At the board level, most of the wiring are direct connections between component pins. The exceptions to this fact are the LCD's display power, Vee, which requires an external potentiometer to function, and the speaker connection, which is simply wire wrapped around the speaker connector jack. The potentiometer hookup for Vee is discribed in appendix A also. Since very few external circuit components are used, a schematic of the component connections will not be provided here. Figure 1 is representative of what the schematics will look like, while Appendix A will provide sufficient pin-out information for the connecting wires.

Microcontroller Design

The HC11 microcontroller is responsible for the following tasks: storing of the actual time, incrementing the time, sending control and display data to the LCD screen, sending the alarm on/off signal, receiving input information from the FPGA, and maintaining the main program loop that calls upon various subroutines according to the input. The main loop handles each task separately through subroutines specific to each task. Each subroutines may use additional function routines that perform special LCD display functions. The following sections describe the software program structure and the input/output port assignments.

Program Structure:

Initialization:

- Clear variables
- Clear Port A and E
- Handshake with FPGA
- Reset Clock, Alarm, and Snooze time to 00:00:00
- Call on subroutine to clear LCD routine

Main Program Loop:

- Jump to subroutine described by MODE variable
- Default to standard mode (MODE0)
- Restart Main program loop

MODE subroutines:

- MODE0 (Standard mode)

- Call on function routine to draw "Standard" screen
- Loop until E (exit) key pressed
 - Call on function to get input from FPGA
 - Update Time if time change
 - Update Time on display
 - Check to see if Alarm triggered
- Write MODE variable and return to Main Program Loop if key pressed
- MODE1 (Time Edit mode)
 - Call on function routine to draw "Time Edit" screen
 - Call on "EDIT" function routine
 - Return to Main Program Loop
- MODE2 (Alarm mode)
 - Calls on function routine to draw "Alarm Edit" screen
 - Loop until E (Edit) or F (exit) key pressed
 - Call on function routine to get input from FPGA
 - Call on function routine to update alarm time
 - Call on function routine to print new alarm time on screen
 Toggles alarm state if key press is A
 - Write MODE variable and returns to Main Program Loop
- MODE3 (Alarm Edit mode)
 - Call on function routine to draw "Alarm Edit" screen
 - Call on EDIT function routine
 - Call on function routine to set snooze time to alarm time
 - Returns to MODE 2

The remainder of the microcontroller code are the function routines which perform

specific tasks such as moving the LCD cursor, or a write to a Time register, etc. Refer to

the code provided in the appendix for more information on these function routines.

FPGA Design

The FPGA is mapped using the Verilog HDL. A total of 5 modules are used. The

following sections describe each module separately.

Main.v:

Inputs: *master_clock, row_data, sound* Outputs: *col_data, number, sclock, change, so_clk*

The main module is the top level module responsible for I/O to other components and wiring between sub-modules.

The *master_clock* signal is generated by an external oscillator. This signal is also the primary clock for the FPGA. With the exception to the *number* bus and *change* pin, all other I/O busses and pins are directly connected to sub-modules.

The 4-bit wide *number* bus and the *change* pin is connected to registers that update with every key press. The *number* register updates to hold the value of the last key pressed, while the *change* register inverts its value. The *change* pin works as a simple handshaking method for communication with the HC11. Since the *number* register always retains the value of the last key pressed, only a change in the value held by the *change* register will the HC11 recognize the key data as new.

<u>Aux_Clock.v</u>:

Input: *mclk* Output: *aux_clk*

This module generates a auxiliary clock signal which has a cycle time equal to 20,000 cycles of the FPGA's primary clock. The *mclk* pin connects to the *master_clock* pin, while *aux_clk* outputs the generated clock signal to other modules.

The clock divider signal is obtained by using a finite state machine that increments a 14-bit register every *mclk* cycle when the register is less than a decimal value of 10,000, at which point the FSM resets the value of the register and restarts.

Keypad_Scan.v:

Input: *aux_clk, row* Output: *col, key_pressed, data_out*

The Keypad_Scan module performs two tasks. First, it scans and debounces the keypad inputs. Second, it decodes any key press into its binary representation recognizable by the HC11's algorithm.

Keypad scanning is done by alternating pulses sent to each column of the matrix keypad, then reading to see if any keypad row is shorted with the column in question. By identifying the row and columns where the short occurred, it's then possible to distinguish one key from another.

The scanning procedure uses a finite state machine. In the starting state, the output to the keypad columns cycles through with every *aux_clk* cycle. When a row value change is detected that value is stored and the finite state machine enters the second state (pause state). The second state is simply a pause necessary to debounce a signal. The machine enters the third state at the next clock cycle. If the row value stored has not changed (key is still pressed), the machine decodes the signal and returns to the original state.

<u>S_Clock</u>.v: Input: *mclk* Output: *s_clk*

This module is the same as the *aux_clk* module with the exception that the clock divider counts up to 500,000 to generate a clock signal with a 1 second period. The generated signal is the signal used to increment the actual time value on the HC11.

Sound_Clk.v

Input: mclk, sound Output: so_clk

This module generates the sound signal sent to the computer speakers. The module nearly the same as *aux_clk* module, but with a divisor of 500 to generate a 1kHz signal, and also the generate signal is "AND'ed" with a *sound*. The *sound* wire effectively serves as a switch to turn the output signal on and off.

Results

The alarm clock worked as planned. All the important aspects of a good alarm

clock - its timing accuracy, functionality, ease of use, etc are all represented in the final

prototype. The LCD alarm clock even feature a user-friendly menu system for time

changes. In short, all the goals set during the planning of this project were met. The only

difficulty in the project occurred when the manufacturer's initialization sequence failed to

work. This was fixed by using another algorithm provided by internet resources.

References

- 1. Burian, Christopher J. "LCD Technical FAQ", http://www.repairfaq.org/filipg/LINK/F_Tech_LCD.html, 1996
- 2. "LCD (programming & pinouts)", http://www.repairfaq.org/filipg/LINK/F_LCD_progr.html, 1996

* Additional sources for LCD projects can be found at http://www.eio.com/lcdintro.htm

Parts List

1. LCD Module

2. PC Speakers

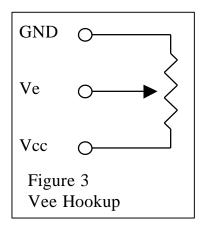
Engineering Stockroom Microprocessor Lab

APPENDIX A

Component Pinouts

- L = LCD Display
- F = FPGA Board
- H = HC11
- K = Keypad
- S = Computer External Speakers
- 1. LCD

L1	GND	GND
L2	Vcc	+5V
L3	Ve	see Figure 3
L4	RS	H28
L5	R/W	H29
L6	E	H30
L7	Data 0	H42
L8	Data 1	H41
L9	Data 2	H40
L10	Data 3	H39
L11	Data 4	H38
L12	Data 5	H37
L13	Data 6	H36
L14	Data 7	H35



2. FPGA

F13	MCLK	Clock
F38	row 0	K 1
F39	row 1	K4
F40	row 2	K5
F44	row 3	K3
F45	col 3	K8
F46	col 2	K7
F47	col 1	K6
F48	col 0	K2
F72	number 0	H44
F77	number 1	H49
F78	number 2	H47
F79	number 3	H45
F81	change	H46
F82	sclock	H43
F83	so_clk	S 3
F84	sound	H27

3. Keypad

K1	row 0	F38
K2	col 0	F48
K3	row 3	F44
K4	row 1	F39
K5	row 2	F40
K6	col 1	F47
K7	col 2	F46
K8	col 3	F45

4. Computer External Speakers

S 1	GND	Ground
S 2	L Speaker	Not Used
S 3	R Speaker	F83

APPENDIX B

HC11 ASM Code

* * * * E157 - Microprocessor-Based Systems * * Final Project - Alarm/Clock with LCD ** * * * * Authors: Jason Fong * * * * Fernando Mattos ** Data Section * * **** Constants **** ZERO EOU \$0000 Used for comparison DELAY EOU \$0002 # of ms for delay. Used in WAIT subroutine **** Time **** Note: All digits in TIME, ALARM and SNOOZE start with \$3 **** Thus, 1 would be \$31 TIME EOU \$0003 Actual time. 6 bytes long. ALARM \$0009 Time for alarm. Same as above EOU \$000F Time for snooze, initially equal to ALARM SNOOZE EOU **** Control MODE EQU \$0015 Mode (0-Time/1-Ed.Time/2-Alarm/3-Ed.Alarm) \$0016 Contains last state of 1sec clock given by FPGA CLOCK EQU CHANGE EQU \$0017 Used to control change in key pressed \$0018 State of alarm (turned ON=1/OFF=0) \$0019 When editing/updating time. 6 bytes long. A_STATE EQU NEW_T EQU \$0020 Digit of NEW_T being edited EDIT_DI EQU EDIT_C EQU \$0021 Edit control (0=Time/1=Alarm) **** Communications **** PORTA EQU \$1000 Output for LCD control PORTB \$1004 Output for LCD data EQU PORTE \$100A EOU Input from FPGA. 0->Second. 1-4->Key. 5->Change ***** ** Program Section * * ORG \$C000 Clears the ZERO variable CLR ZERO CLR ZERO+1 CLR MODE Goes to mode 0 (normal operation) CLR CLOCK Sets clock to 0 (arbitrary) LDAA #\$00 STAA PORTA Erases all bits in PORTA => Turns off alarm LDAA PORTE Loads PORTE ANDA #\$20 Leaves only bit 5 (change)

STAA CHANGE Sets CHANGE to the value at the FPGA LDAA #\$30 Resets TIME, ALARM and SNOOZE to 00:00:00 STAA TIME STAA ALARM STAA SNOOZE STAA TIME+1 STAA ALARM+1 STAA SNOOZE+1 STAA TIME+2 STAA ALARM+2 STAA SNOOZE+2 STAA TIME+3 STAA ALARM+3 STAA SNOOZE+3 STAA TIME+4 STAA ALARM+4 STAA SNOOZE+4 STAA TIME+5 STAA ALARM+5 SNOOZE+5 STAA INITDR Initialization of LCD driver JSR JSR CLEAR Clear LCD screen JSR CUR_OFF Turns cursor OFF MLOOP MODE Checks which mode of operation is active LDAA CMPA #\$00 BNE M1 MODE0 Mode 0 - Show time JSR ENDLOOP JMP CMPA #\$01 BNE М2 Mode 1 - Edit time JSR MODE1 ENDLOOP JMP #\$02 CMPA BNE МЗ JSR MODE 2 Mode 2 - Show alarm JMP ENDLOOP CMPA #\$03 BNE NONE JSR MODE 3 Mode 3 - Edit Alarm ENDLOOP JMP NONE Default -> Go to mode 0 CLRMODE ENDLOOP JMP MLOOP SWI

*** Function to initialize LCD driver

M1

М2

M3

*** Commands done as explained in LCD spec sheet

ORG \$C100 INITDR LDAA #\$38 JSR WRITEC LDAA #\$38 JSR WRITEC LDAA #\$38 JSR WRITEC LDAA #\$06 JSR WRITEC LDAA #\$0C JSR WRITEC RTS *** Function to write control information to LCD *** Control data in register A ORG \$C180 WRITEC * Bit 5 -> R/W, Bit 4 -> RS, Bit 3 -> E LDAB PORTA #%11000111 R/W=0,RS=0,E=0 ANDB STAB PORTA STAA PORTB Write controls LDAB PORTA #%11001111 ANDB ORAB #%00001000 R/W=0,RS=0,E=1 STAB PORTA LDAB PORTA ANDB #%11000111 R/W=0,RS=0,E=0STAB PORTA LDAB PORTA R/W=1,RS=0,E=0 ANDB #%11100111 ORAB #%00100000 STAB PORTA LDAA #10 Delay for 10ms STAA DELAY JSR WAIT RTS *** Function to write character data to LCD *** Character data in register A ORG \$C200 WRITED LDAB PORTA ANDB #%11010111 R/W=0,RS=1,E=0 #%00010000 ORAB STAB PORTA Write character STAA PORTB LDAB PORTA ANDB #%11011111 R/W=0,RS=1,E=1 ORAB #%00011000 STAB PORTA LDAB PORTA ANDB #%11010111 R/W=0,RS=1,E=0 ORAB #%00010000 STAB PORTA LDAB PORTA

ANDB #%11110111 R/W=1,RS=1,E=0 ORAB #%00110000 STAB PORTA LDAA #2 Delay for 2ms STAA DELAY JSR WAIT RTS *** Function to clear LCD screen ORG \$C280 CLEAR LDAA #\$01 JSR WRITEC RTS *** Function to turn cursor on ORG \$C300 CUR_ON LDAA #\$0D JSR WRITEC RTS *** Function to turn cursor off ORG \$C380 CUR_OFF LDAA #\$0C WRITEC JSR RTS *** Function to move cursor one space to left \$C400 ORG CUR_LEFT #\$10 LDAA JSR WRITEC RTS *** Function to move cursor one space to right ORG \$C480 CUR_RIGHT #\$14 LDAA JSR WRITEC RTS *** Function to move cursor to a column in row 1 *** Column in register A ORG \$C500 CUR1 DECA ADDA #\$80 WRITEC JSR RTS *** Function to move cursor to a column in row 2 $\,$ *** Column in register A ORG \$C580 CUR2 DECA

ADDA #\$C0 WRITEC JSR RTS *** Function to move cursor to a column in row 3 *** Column in register A ORG \$C600 CUR3 DECA ADDA #\$94 JSR WRITEC RTS *** Function to move cursor to a column in row 4 *** Column in register A ORG \$C680 CUR4 DECA ADDA #\$D4 JSR WRITEC RTS *** Function to move cursor home (0,0) ORG \$C700 HOME LDAA #\$02 JSR WRITEC RTS *** Operation Mode 0 ORG \$C780 MODE 0 SCREENO Draw screen for mode 0 JSR LOOPO GINPUT Update time and get input. A=Key. B<>0 for JSR keypress PSHA PSHB JSR TIME2NEWT JSR PRTIME Print time JSR CK_ALARM #\$00 CMPB BNE M01 Redraws screen PULB PULA CMPB #\$00 LOOPO No key pressed... keep waiting BEQ CMPA #\$0A BNE MOKE LDAA #\$02 STAA MODE JMP ENDM0 MOKE CMPA #\$0E BNE LOOP0

LDAA #\$01 STAA MODE JMP ENDM0 M01 PULB PULA JMP MODE0 ENDM0 RTS *** Draw screen for mode 0 ORG \$C900 SCREEN0 JSR CLEAR LDAA #8 "Time" on col 8, row 1 JSR CUR1 #\$54 LDAA JSR WRITED #\$69 LDAA WRITED JSR LDAA #\$6D JSR WRITED LDAA #\$65 JSR WRITED "Alarm" on col 6, row 3 LDAA #6 JSR CUR 3 LDAA #\$41 JSR WRITED LDAA #\$6C JSR WRITED #\$61 LDAA JSR WRITED LDAA #\$72 JSR WRITED #\$6D LDAA JSR WRITED "ON" or "OFF" on col 12, row 3 LDAA #12 CUR3 JSR LDAA #\$4F JSR WRITED LDAA A_STATE CMPA #\$01 BNE S0_AOFF Alarm is OFF #\$4E LDAA JSR WRITED JMP S0_1 S0_AOFF LDAA #\$46 JSR WRITED LDAA #\$46 JSR WRITED S0_1

	LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR	#1 CUR4 #\$45 WRITED #\$80 WRITED #\$45 WRITED #\$64 WRITED #\$69 WRITED #\$74 WRITED	"E-Edit"	
	LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR	#14 CUR4 #\$41 WRITED #\$80 WRITED #\$41 WRITED #\$6C WRITED #\$61 WRITED #\$72 WRITED #\$6D WRITED	"A-Alarm"	
*** Opei	ration Mo ORG	ode 1 \$CA00		
MODE1	JSR LDAA STAA	SCREEN1 #\$00 EDIT_C	Draw screen i	for mode 1
	JSR LDAA STAA	EDIT #\$00 MODE		
	RTS			
*** Drav SCREEN1	w screen ORG	for mode \$CB00	2 1	
	JSR	CLEAR		
	LDAA JSR	#6 CUR1 #\$45 WRITED #\$64	"Edit Time" d	on col 6, row 1

JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR	WRITED #\$69 WRITED #\$74 WRITED #\$FE WRITED #\$54 WRITED	
LDAA JSR	#\$69 WRITED	
LDAA	#\$6D	
JSR	WRITED	
LDAA	#\$65	
JSR	WRITED	
LDAA	#1	"A-Left"
JSR	CUR4	
LDAA	#\$41	
JSR	WRITED	
LDAA	#\$ВО	
JSR	WRITED	
LDAA	#\$4C	
JSR	WRITED	
LDAA	#\$65	
JSR	WRITED #\$66	
LDAA JSR	#Ş00 WRITED	
LDAA	#\$74	
JSR	WRITED	
LDAA	#\$FE	
JSR	WRITED	
LDAA	#\$42	"B-Right"
JSR	WRITED	2
LDAA	#\$ВО	
JSR	WRITED	
LDAA	#\$52	
JSR	WRITED	
LDAA	#\$69	
JSR	WRITED	
LDAA	#\$67	
JSR	WRITED	
LDAA	#\$68 WRITED	
JSR LDAA	#\$74	
JSR	#Ş/4 WRITED	
LDAA	#\$FE	
JSR	WRITED	
LDAA	#\$46	"F-Ret"
JSR	WRITED	
LDAA	#\$ВО	
JSR	WRITED	
LDAA	#\$52	
JSR	WRITED	
LDAA	#\$65	
JSR	WRITED	
LDAA	#\$74	

JSR WRITED RTS *** Operation Mode 2 ORG \$CC00 MODE 2 JSR SCREEN2 Draw screen for mode 2 LOOP2 GINPUT Update time and get input. A=Key. B<>0 for JSR keypress PSHA PSHB JSR ALARM2NEWT JSR PRTIME Print time PULB PULA CMPB #\$00 BEQ LOOP2 No key pressed... keep waiting CMPA #\$0F BNE M2KA #\$00 LDAA MODE STAA JMP ENDM2 M2KA CMPA #\$0A BNE M2KE LDAA A_STATE CMPA #\$01 BNE M2KA1 LDAA #\$00 STAA A_STATE MODE 2 JMP M2KA1 #\$01 LDAA STAA A_STATE JMP MODE2 M2KE CMPA #\$0E BNE LOOP2 #\$03 LDAA STAA MODE ENDM2 RTS *** Draw screen for mode 2 \$CD00 ORG SCREEN2 JSR CLEAR LDAA #7 "Alarm" on col 7, row 1 JSR CUR1 #\$41 LDAA WRITED JSR

LDAA #\$6C JSR WRITED LDAA #\$61 JSR WRITED #\$72 LDAA JSR WRITED LDAA #\$6D WRITED JSR LDAA #6 "Alarm" on col 6, row 3 JSR CUR3 LDAA #\$41 JSR WRITED LDAA #\$6C JSR WRITED LDAA #\$61 JSR WRITED #\$72 LDAA JSR WRITED LDAA #\$6D JSR WRITED "ON" or "OFF" on col 12, row 3 LDAA #12 JSR CUR3 LDAA #\$4F JSR WRITED LDAA A STATE CMPA #\$01 BNE S2_AOFF Alarm is OFF LDAA #\$4E JSR WRITED JMP S2_1 S2_AOFF LDAA #\$46 JSR WRITED #\$46 LDAA JSR WRITED S2 1 #1 "A-ON/OFF" LDAA JSR CUR4 LDAA #\$41 JSR WRITED #\$ВО LDAA JSR WRITED LDAA #\$4F JSR WRITED LDAA #\$4E JSR WRITED #\$2F LDAA JSR WRITED LDAA #\$4F JSR WRITED LDAA #\$46 JSR WRITED LDAA #\$46 JSR WRITED LDAA #\$FE

	LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA	WRITED #\$B0 WRITED #\$45 WRITED #\$64 WRITED #\$69 WRITED #\$74 WRITED #\$FE WRITED #\$46 WRITED	"E-Edit" "F-Ret"
	RTS		
*** Ope: MODE3	ration Mo ORG	ode 3 \$CE00	
	JSR LDAA STAA	SCREEN3 #\$01 EDIT_C	Draw screen for mode 3
	JSR	EDIT	
	JSR	ALARM2SN	JOOZE
	LDAA STAA	#\$02 MODE	
	RTS		
*** Dra	w screen	for mode	2 3
SCREEN3	ORG	\$CF00	
Dentering	JSR	CLEAR	
	LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA	#6 CUR1 #\$45 WRITED #\$64 WRITED #\$69 WRITED #\$74 WRITED #\$FE	"Edit Alarm" on col 6, row 1

JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR	WRITED #\$41 WRITED #\$6C WRITED #\$61 WRITED #\$72 WRITED #\$6D WRITED	
LDAA	#1	"A-Left"
JSR	CUR4	
LDAA	#\$41	
JSR	WRITED	
LDAA	#\$ВО	
JSR	WRITED	
LDAA	#\$4C	
JSR	WRITED	
LDAA	#\$65	
JSR	WRITED	
LDAA	#\$66	
JSR	WRITED	
LDAA JSR	#\$74 WRITED	
LDAA	#\$FE	
JSR	WRITED	
LDAA	#\$42	"B-Right"
JSR	WRITED	2
LDAA	#\$ВО	
JSR	WRITED	
LDAA	#\$52	
JSR	WRITED	
LDAA	#\$69	
JSR	WRITED	
LDAA	#\$67	
JSR	WRITED	
LDAA JSR	#\$68 WRITED	
LDAA	#\$74	
JSR	WRITED	
LDAA	#\$FE	
JSR	WRITED	
LDAA	#\$46	"F-Ret"
JSR	WRITED	
LDAA	#\$ВО	
JSR	WRITED	
LDAA	#\$52	
JSR	WRITED	
LDAA JSR	#\$65 WRITED	
LDAA	#\$74	
JSR	#Ş/4 WRITED	
RTS		
-		

CINDUM	ORG	\$D400	
GINPUT	LDAA PSHA	PORTE	
	ANDA	#\$01 CLOCK	Deletes all bits but bit 0
	BEQ	NOUPD CLOCK	No change => No update
	CMPA	#\$01	
	BNE JSR	NOUPD INCTIME	Updates only on rising edge of clock
NOUPD			
	PULA PSHA		
	ANDA	#\$20	Deletes all bits but bit 5
	CMPA BEQ	CHANGE NOKEY	No key pressed
	-	CHANGE	
	LDAB	#\$01	Store 1 in B to indicate key pressed
	PULA ANDA	#\$1E	Deletes all bits but bit 1-4
	LSRA		Shifts 1 bit to right. $A = Key pressed$
	JMP	ENDGIN	
NOKEY			
	PULA CLRB		Clear register B to indicate no key pressed
			clear register b to marcate no key pressed
ENDGIN	RTS		
**** ጥፖ	ansfer Al	LAPM to 9	SNOOZE
11	ORG	\$D4B0	510021
ALARM2S			
	LDAA		
		ALARM	
	STAA	SNOOZE	
	STAA LDAA	SNOOZE ALARM+1	1
	STAA LDAA STAA	SNOOZE ALARM+1 SNOOZE+3	1
	STAA LDAA STAA LDAA	SNOOZE ALARM+1 SNOOZE+3 ALARM+2	
	STAA LDAA STAA LDAA STAA	SNOOZE ALARM+1 SNOOZE+2 ALARM+2 SNOOZE+2	2
	STAA LDAA STAA LDAA STAA LDAA	SNOOZE ALARM+1 SNOOZE+2 ALARM+2 SNOOZE+2 ALARM+3	2
	STAA LDAA STAA LDAA STAA LDAA STAA	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+:	2
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA	SNOOZE ALARM+1 SNOOZE+2 ALARM+2 SNOOZE+2 ALARM+3 SNOOZE+2 ALARM+4	2 3
	STAA LDAA STAA LDAA STAA LDAA STAA STAA	SNOOZE ALARM+1 SNOOZE+ ALARM+2 SNOOZE+ ALARM+3 SNOOZE+ ALARM+4 SNOOZE+	2 3
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA	SNOOZE ALARM+1 SNOOZE+ ALARM+2 SNOOZE+ ALARM+3 SNOOZE+ ALARM+4 SNOOZE+ ALARM+5	2 3 4
	STAA LDAA STAA LDAA STAA LDAA STAA STAA	SNOOZE ALARM+1 SNOOZE+ ALARM+2 SNOOZE+ ALARM+3 SNOOZE+ ALARM+4 SNOOZE+	2 3 4
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA STAA	SNOOZE ALARM+1 SNOOZE+ ALARM+2 SNOOZE+ ALARM+3 SNOOZE+ ALARM+4 SNOOZE+ ALARM+5	2 3 4
**** Tr	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+: ALARM+4 SNOOZE+: SNOOZE+: SNOOZE+:	2 3 4 5
**** Tr TIME2NE	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS ansfer T: ORG	SNOOZE ALARM+1 SNOOZE+ ALARM+2 SNOOZE+ ALARM+3 SNOOZE+ ALARM+4 SNOOZE+ ALARM+5 SNOOZE+	2 3 4 5
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS ansfer T: ORG	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+: ALARM+4 SNOOZE+: ALARM+5 SNOOZE+: SNOOZE+:	2 3 4 5
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS ansfer T: ORG WT LDAA	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+: ALARM+4 SNOOZE+: ALARM+5 SNOOZE+: IME to NI \$D500 TIME	2 3 4 5
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS ansfer T: ORG	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+: ALARM+4 SNOOZE+: ALARM+5 SNOOZE+: SNOOZE+:	2 3 4 5
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS ansfer T: ORG WT LDAA STAA	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+: ALARM+4 SNOOZE+: ALARM+5 SNOOZE+: IME to NI \$D500 TIME NEW_T	2 3 4 5
	STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA LDAA STAA RTS ORG WT LDAA STAA LDAA STAA LDAA	SNOOZE ALARM+1 SNOOZE+: ALARM+2 SNOOZE+: ALARM+3 SNOOZE+: ALARM+4 SNOOZE+: ALARM+5 SNOOZE+: IME to NI \$D500 TIME NEW_T TIME+1	2 3 4 5

STAA NEW T+2 LDAA TIME+3 STAA NEW_T+3 LDAA TIME+4 STAA NEW_T+4 LDAA TIME+5 STAA NEW T+5 RTS **** Transfer NEW T to TIME ORG \$D540 NEWT2TIME LDAA NEW_T STAA TIME LDAA NEW_T+1 STAA TIME+1 LDAA NEW T+2 STAA TIME+2 LDAA NEW_T+3 STAA TIME+3 LDAA NEW T+4 TIME+4 STAA NEW_T+5 LDAA STAA TIME+5 RTS **** Transfer SNOOZE to NEW T ORG \$D580 SNOOZE2NEWT LDAA SNOOZE STAA NEW_T SNOOZE+1 LDAA NEW_T+1 STAA LDAA SNOOZE+2 STAA NEW_T+2 LDAA SNOOZE+3 NEW T+3 STAA LDAA SNOOZE+4 NEW_T+4 STAA SNOOZE+5 LDAA STAA NEW T+5 RTS **** Transfer NEW T to SNOOZE ORG \$D5B0 NEWT2SNOOZE LDAA NEW_T STAA SNOOZE LDAA NEW_T+1 STAA SNOOZE+1 LDAA NEW_T+2 STAA SNOOZE+2 LDAA NEW T+3 STAA SNOOZE+3 LDAA NEW T+4 STAA SNOOZE+4 LDAA NEW_T+5

STAA SNOOZE+5 RTS **** Transfer ALARM to NEW_T ORG \$D600 ALARM2NEWT LDAA ALARM STAA NEW T LDAA ALARM+1 STAA NEW_T+1 ALARM+2 LDAA STAA NEW_T+2 LDAA ALARM+3 STAA NEW_T+3 LDAA ALARM+4 STAA NEW_T+4 LDAA ALARM+5 STAA NEW_T+5 RTS **** Transfer NEW_T to ALARM ORG \$D640 NEWT2ALARM LDAA NEW_T STAA ALARM LDAA NEW_T+1 STAA ALARM+1 LDAA NEW T+2 STAA ALARM+2 NEW_T+3 LDAA ALARM+3 STAA LDAA NEW_T+4 STAA ALARM+4 LDAA NEW T+5 STAA ALARM+5 RTS **** Function to increment 1s to TIME ORG \$D680 INCTIME JSR TIME2NEWT JSR INCREM Increments 1 second to NEW_T NEWT2TIME JSR RTS **** Function to increment 5min to SNOOZE ORG \$D6B0 INCSNOOZE JSR SNOOZE2NEWT CLRA INCSLOOP PSHA JSR INCREM PULA INCA CMPA #180

BNE INCSLOOP JSR NEWT2SNOOZE RTS **** Function to increment 1s to NEW_T \$D700 ORG INCREM NEW_T+5 Load least sig. digit of the seconds LDAA CMPA #\$39 BEQ INCT1 INCA STAA NEW_T+5 JMP ENDINCT INCT1 LDAA #\$30 STAA NEW_T+5 LDAA NEW_T+4 CMPA #\$35 BEQ INCT2 INCA STAA NEW_T+4 ENDINCT JMP INCT2 #\$30 LDAA NEW_T+4 STAA NEW_T+3 LDAA #\$39 CMPA BEQ INCT3 INCA NEW_T+3 STAA JMP ENDINCT INCT3 #\$30 LDAA STAA NEW T+3 LDAA NEW_T+2 CMPA #\$35 BEQ INCT4 INCA STAA NEW_T+2 ENDINCT JMP INCT4 LDAA #\$30 STAA NEW_T+2 LDAA NEW_T+1 LDAB NEW_T CMPB #\$32 BEQ INCT5 CMPA #\$39 BEQ INCT6 INCA STAA NEW T+1 JMP ENDINCT INCT5 CMPA #\$33 INCT7 BEQ

INCA STAA NEW_T+1 JMP ENDINCT INCT6 #\$30 LDAA NEW_T+1 STAA INCB NEW_T STAB JMP ENDINCT INCT7 LDAA #\$30 STAA NEW_T+1 LDAB #\$30 STAB NEW_T ENDINCT RTS **** Function to print time (NEW_T) on LCD (Start on ROW 2, COL 5) \$D800 ORG PRTIME #6 Jump to Row 2, Col 6 LDAA JSR CUR2 LDAA NEW_T JSR WRITED LDAA NEW T+1 JSR WRITED Print ":" LDAA #\$3A JSR WRITED LDAA NEW_T+2 JSR WRITED NEW_T+3 LDAA JSR WRITED #\$3A Print ":" LDAA WRITED JSR NEW T+4 LDAA JSR WRITED NEW_T+5 LDAA WRITED JSR RTS **** Function to edit NEW_T ORG \$D900 EDIT CLR EDIT_DI Starts editing digit 0 CLRB TIME2NEWT JSR LDAA EDIT_C CMPA #0 LOOPET BEQ JSR ALARM2NEWT LOOPET

PSHA PSHA PSHA PSHA PSHB LDAA EDIT_C CMPA #1 BEQ ET2 JSR TIME2NEWT JSR ALARM2NEWT ET3 JSR ET3 JSR JSR PRTIME PSFIME Print time LDAA #6 Erase everything on row 3 JSR CUR3 LDAA #\$FE JSR WRITED LDAA #\$FE
PSHB LDAA EDIT_C CMPA #1 EEQ ET2 JSR TIME2NEWT JSR ALARM2NEWT ET3 JSR ALARM2NEWT ET3 JSR PRTIME Print time LDAA #6 Erase everything on row 3 JSR CUR3 LDAA #5FE JSR WRITED LDAA #5FE JSR WRITED
CMPA #1 BEQ ET2 JSR TIME2NEWT JMP ET3 ET2 JSR ALARM2NEWT ET3 JSR PRTIME Print time LDAA #6 Erase everything on row 3 JSR CUR3 LDAA #\$FE JSR WRITED LDAA #\$FE JSR WRITED
BEQ ET2 JSR TIME2NEWT TIME2NEWT ET2 DSR ALARM2NEWT ET3 JSR PRTIME Print time LDAA #6 Erase everything on row 3 JSR CUR3 LDAA #\$FE JSR WRITED LDAA #\$FE
JSR TIME2NEWT JSR TIME2NEWT TT2 T2 JSR ALARM2NEWT T3 JSR PRTIME Print time LDAA #6 Erase everything on row 3 JSR CUR3 LDAA #5FE JSR WRITED
JMP ET3 ET3 JSR ALARM2NEWT ET3 JSR PRTIME JSR PRTIME Print time LDAA # 6 Erase everything on row 3 JSR CUR3 LDAA JSR WRITED JSR JDAA #\$FE JSR JSR WRITED JSR JSR WRITED
ET2 T3 T3 T4 T5
ET3 JSR ALARM2NEWT ET3 JSR PRTIME JSR PRTIME Print time LDAA #6 Erase everything on row 3 JSR CUR3 IDAA LDAA #\$FE JSR JSR WRITED IDAA LDAA #\$FE IDAA
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LDAA #\$FE
JSR WRITED
LDAA #\$FE JSR WRITED
LDAA #6 Jumps to col correct column, row 2
LDAB EDIT_DI
CMPB #4
BLO ETO
INCA
ETO
CMPB #2
BLO ET1 INCA
ET1
ADDA EDIT_DI
JSR CUR3
LDAA #\$5E
JSR WRITED
PULB
PULA
CMPB #\$00
BEQ LOOPET No key pressed keep waiting
CMPA #\$0A "A" pressed -> Move left
BNE ET5
LDAB EDIT_DI
CMPB #0

	BEQ	ET4					
	DECB STAB JMP	EDIT_DI LOOPET					
ET4	LDAB STAB JMP	#5 EDIT_DI LOOPET					
ET5							
	CMPA BNE LDAB CMPB BEQ INCB STAB JMP	#\$0B ET7 EDIT_DI #5 ET6 EDIT_DI LOOPET	"B"	pressed	->	Move	right
ET6	TDID						
	LDAB STAB JMP	#0 EDIT_DI LOOPET					
ET7							
	CMPA BNE JMP	#\$0F ET8 ENDET					
ET8							
	LDAB CMPB BEQ CMPB BEQ CMPB BEQ CMPB BEQ CMPB BEQ CMPB BEQ CLR JMP	EDIT_DI #0 ETD0 #1 ETD1 #2 ETD2 #3 ETD2 #3 ETD3 #4 ETD4 #5 ETD5 EDIT_DI LOOPET					
etd0							
ETD01	CMPA BHI ADDA STAA LDAA STAA JMP	#\$02 ETD01 #\$30 NEW_T #1 EDIT_DI ETUPDATE					
	JMP	LOOPET					
ETD1							

	LDAB CMPB BEQ	NEW_T #\$32 ETD11
	CMPA BHI ADDA STAA LDAA STAA JMP	#\$09 ETD12 #\$30 NEW_T+1 #2 EDIT_DI ETUPDATE
ETD11		
	CMPA BHI ADDA STAA LDAA STAA JMP	#\$03 ETD12 #\$30 NEW_T+1 #2 EDIT_DI ETUPDATE
ETD12		
	JMP	LOOPET
ETD2		
ETD21 ETD3 ETD31	CMPA BHI ADDA STAA LDAA STAA JMP JMP CMPA BHI ADDA STAA LDAA STAA JMP JMP	ETUPDATE LOOPET #\$09 ETD31 #\$30 NEW_T+3
etd4	CMPA BHI ADDA STAA LDAA STAA	#\$05 ETD41 #\$30 NEW_T+4 #5 EDIT_DI
ETD41	JMP	ETUPDATE
	JMP	LOOPET
ETD5	CMPA	#\$09

BHI ETD51 ADDA #\$30 STAA NEW_T+5 #0 LDAA STAA EDIT_DI JMP ETUPDATE

ETD51

ETUP1

ENDET

CK ALARM

ENDAL

CK TIME

MP	LOOPET

ETUP1

NEWT2TIME

LOOPET

NEWT2ALARM

**** Function ALARM - Checks if TIME=SNOOZE

LOOPET

**** B=0 if alarm doesn't go off

\$DB00

#0 ENDAL

#\$01

TIME

NEW_T

BNE

JSR

JMP

JSR JMP

RTS

ORG

CLRB LDAA

CMPA

BEO

JSR

JSR CLRB

BNE

JSR LDAB

RTS

ORG

LDAA

LDAB

CMPA

EDIT_C LDAA

CMPA #0

ETUPDATE

JI

CBA BNE ENDCK LDAA TIME+1 NEW_T+1 LDAB CBA

BNE ENDCK TIME+2 LDAA LDAB NEW T+2

CBA BNE ENDCK

LDAA TIME+3

A_STATE Check if ALARM ON/OFF

CK_TIME Checks if TIME=SNOOZE

If ALARM OFF, doesn't check it

Equal... Sounds alarm

#\$01 Puts 1 into B to indicate alarm went off

SNOOZE2NEWT Transfers SNOOZE to NEW_T

ENDAL Not equal... Doesn't sound alarm

**** Function to check if TIME=NEW_T \$DB80

ALARMOFF

LDAB NEW_T+3 CBA BNE ENDCK LDAA TIME+4 LDAB NEW_T+4 CBA BNE ENDCK TIME+5 LDAA NEW_T+5 LDAB CBA BNE ENDCK1 LDAA #\$01 JMP ENDCK ENDCK1 LDAA #\$00 ENDCK RTS **** Function ALARMOFF - Sounds the alarm \$DC00 ORG ALARMOFF PORTA LDAA ORAA #\$40 Turns on alarm STAA PORTA ALSCREEN JSR ALLOOP JSR GINPUT Update time and get input. A=Key. B<>0 for keypress PSHA PSHB JSR TIME2NEWT JSR PRTIME Print time PULB PULA #\$00 CMPB BEQ ALLOOP No key pressed... keep waiting CMPA #\$0A BNE ALOFFB #\$00 LDAA STAA A_STATE JMP ENDALOFF ALOFFB CMPA #\$0B BNE ALLOOP JSR INCSNOOZE ENDALOFF LDAA PORTA ANDA #\$BF Turns off alarm STAA PORTA RTS

**** Funct OR		N - Draws screen for alarm off
ALSCREEN		
JS	R CLEAR	
LD	AA #3	"Go to MicroPs" on col 3, row 1
	R CUR1	
	AA #\$47	
JS		D
	AA #\$6F	
	SR WRITED	D
	AA #\$FE	
	R WRITED	ח
	AA #\$74	-
	R WRITED	ח
	AA #\$6F	-
	R WRITED	ח
	AA #\$FE	
	R WRITED	D
	AA #\$4D	
	R WRITED	D
	AA #\$69	-
	R WRITED	D
	AA #\$63	-
	R WRITED	ס
	AA #\$72	-
JS		D
	AA #\$6F	-
	R WRITED	D
	AA #\$50	
	R WRITED	D
	AA #\$73	
JS		D
LD	AA #2	">>>"
JS	R CUR2	
LD	AA #\$3E	
JS	R WRITED	D
LD	AA #\$3E	
JS		D
	AA #\$3E	
JS		D
LD	AA #15	" <<< "
JS	R CUR2	
	AA #\$3C	
JS		D
	AA #\$3C	
JS		D
	AA #\$3C	
JS	R WRITED	D
	AA #1	"A-Turn Alarm OFF"
JS		
	AA #\$41	
JS	R WRITED	

JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR	WRITED #\$54 WRITED #\$75 WRITED #\$62 WRITED #\$62 WRITED #\$62 WRITED #\$41 WRITED #\$60 WRITED #\$61 WRITED #\$61 WRITED #\$62 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED #\$60 WRITED		
JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR LDAA JSR	WRITED #1 CUR4 #\$42 WRITED #\$60 WRITED #\$65 WRITED #\$6F WRITED #\$6F WRITED #\$65 WRITED #\$65 WRITED #\$7A WRITED #\$78 WRITED #\$65 WRITED #\$28 WRITED #\$33 WRITED #\$60 WRITED #\$69	"B-Snooze	(3min)"

JSR WRITED LDAA #\$6E JSR WRITED LDAA #\$29 JSR WRITED RTS **** Function WAIT1 - For one milisecond delay ORG \$DE80 WAIT1 LDY #40 Cycles for a total of 120 LOOPW1 DEY Decrements Y CPY ZERO Compares Y with ZERO (2 bytes) BNE LOOPW1 If not zero, loop LDY #40 LOOPW2 DEY Repeats above 3 times -> Sums up to about 1 ms CPY ZERO BNE LOOPW2 LDY #40 LOOPW3 DEY ZERO CPY LOOPW3 BNE RTS Returns to WAIT subroutine **** Function WAIT - For variable amount of seconds \$DF00 ORG WAIT LDAA DELAY Loads DELAY into the A register LOOPW CMPA ZERO Compares with zero BEQ RETURN If equal, return to main routine JSR WAIT1 Else, wait 1 ms DECA Decrements A JMP LOOPW Loops RETURN RTS

END

APPENDIX C

FPGA Verilog Files

APPENDIX D

LCD Spec Sheets

Please refer to

http://www.optrex.co.jp/us/lcd_us/index.html

for the latest information on Optrex LCD information