# Microprocessor-Based Systems (E155)

**Harris** **Fall 2006**

Syllabus

## Contact Information

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|---|---|---|---|---|---|
| Instructor: | David Harris | Parsons 2374 | x73623 | David_Harris@hmc.edu | |
| Lab Assistant: | Carl Nygaard | | x71431 | cnygaard@hmc.edu | Sat 1-3 |
| | Chris Woodruff | | x70503 | cwoodruff@hmc.edu | Sun TBD |
| Class web page: | www3.hmc.edu/~harris/class/e155 | | | | |
| Class directory: | \\Charlie\Courses\Engineering\E155 | | | | |
| Class email list: | eng-155-l | | | | |

Be sure to check that you are on the class email list. You should have received email before the beginning of classes. If you did not receive mail, add yourself to the list or risk missing important late-breaking announcements. To subscribe, send email to listkeeper@hmc.edu with one line in the body:

```
subscribe eng-155-l
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## Schedule

| | |
|---|---|
| Lecture: | MW 1:15-2:30 |
| Lab: | M 2:45 – 5:15 / T 1:15-3:45 |
| Office Hours: | TBD |

You will be working on labs on your own time and it is not required that you attend the entire scheduled lab period. However, you should plan to show up for the first few minutes of each lab to see demonstrations. You also must get your projects checked off at some point during the lab period.

You are encouraged to come to office hours to ask questions, get help with your labs, talk about careers and grad schoo, or just raid the candy jar. Even if I am not officially holding office hours, I am available more often than not, so try dropping in if you are having a problem with your lab. You may also contact the lab assistants for questions when I am not available.

## Recommended Texts

The following texts are not required, but you may find them useful, especially if you are considering employment in the area of digital systems. Some books are also on reserve at Sprauge.

Wakerley, *Digital Design, Principles & Practice*,4rd Edition, Prentice Hall.
A comprehensive text on digital design with lots of useful tips.
Smith and Frazon, *Verilog Styles for Synthesis*, Prentice Hall.
Covers Verilog syntax and style issues in more depth than the class notes.

## Grading

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|---|---|
| Labs: | 50% |
| Final Project: | 45% |
| Activities: | 5% |

Your grade in the class is based on seven labs and a final project. Late labs are not accepted, but your lowest lab score will be dropped before the average is calculated so if you are sick or have an emergency one week you can drop that lab. Labs are done individually. You are welcome to discuss them with other students or the instructor after you have made an effort by yourself. Please list the names of other students you have worked with. However, you should turn in your own work, not work identical to that of another person. **It is an honor code violation to simply copy someone else's work.** Solutions to past years labs have been handed out. Obviously, it is also an honor code violation to refer to these solutions while doing your lab. The final project will be done in groups of two.

Wednesday lectures will consist of in-class activities and design projects. Your work will count toward a small portion of your grade. Your two activitiy lowest scores will be dropped.

## Schedule

| Week | Monday Lecture | Wednesday Activity | Lab Demo | Due |
|---|---|---|---|---|
| **8/28** | | Class Intro | no lab | |
| **9/4** | Comb & Seq Logic | Logic Design | Xilinx Schematics | |
| **9/11** | Verilog 1 | FPGA Datasheet | FPGA Board | Lab 1 |
| **9/18** | Verilog 2 | Verilog Coding | Xilinx Verilog | Lab 2 |
| **9/25** | Synchronous Design | Verilog FSMs | Logic Analyzer | Lab 3 |
| **10/2** | PIC Assembly | PIC Programming | PIC ICD | Lab 4 |
| **10/9** | PIC Hardware | PIC Interfacing | PIC Interfacing | Lab 5 |
| **10/16** | **Fall Break: No Class** | | | |
| **10/23** | C Programming | C Examples | C Programming | Lab 6 |
| **10/30** | **Project Kickoff: No Class** | | | |
| **11/6** | <Topic 1> | Patent Law (seminar, 4:15) | | Lab 7, Project Proposal |
| **11/13** | Interview Questions | <Topic 2> | | |
| **11/20** | Presentations | Presentations | | Project Status Report |
| **11/27** | Presentations | No lecture | | |
| **12/4** | Computer Eng. Jobs | Project Demos | | Report Due 12/7 |