Microprocessor-Based Systems (E155)

Harris **Fall 2004**

Final Project Requirements

Overview

The E155 Final Project is a chance for you to apply your new skills in digital design to a moderate sized problem as part of a two-person team. You should begin thinking about a project and teammate right away. Your project has the following milestones:

11/8:	Project Proposal Due
11/22:	Project Status Report Due
11/22-24:	Project Presentations
12/6-12/7:	Project Demonstrations
12/9:	Final Report Due

Project Suggestions

Be creative when selecting your project. Your project should be bigger than a 1-week lab assignment, but small enough to be doable. If in doubt, err on the side of smaller. You will fail the class if you underake a project that is too big and produce no completed work.

I expect a typical project will use both the FPGA and PIC. It should require at least 3 of the following features:

- A/D converter
- D/A converter
- Timer
- Serial communication with a host PC
- Interfacing with a PC running LabView
- EEPROM
- Interrupts
- Pulse accumulator
- Custom-made PC board

- External RAM
- Compiled C code

However, I will consider other projects that are unique and require adequate technical work, even if they only involve one chip. Some possible examples include:

- A subsystem of your clinic project (with approval of your clinic advisor)
- Experiments with the PIC microcontroller for future E155 labs
- A product for a startup company
- A demonstration of metastability in digital systems
- An improved E155 utility board
- A microprocessor on your FPGA implementing a subset of the PIC ISA
- Control of an electromechanical system
- Interfacing your hardware to a VGA monitor
- Interfacing your hardware to an LCD display and keypad
- A large digital design built on a million gate Virtex FPGA (check the FPGA board out from the stockroom)
- A simple video game

You can find examples of past final projects on the class web page. If you want to choose a project not meeting these typical specifications, be certain to contact the instructor before your submit your proposal.

Budget

If your team needs parts that are not available in the stockroom, you may spend up to $50 to purchase them. You will need to save your receipts, fill out a reimbursement form in the department office, and have me sign the form. Of course, you can exceed this budget, but you must pay the remainder out of your own pocket.

Deliverables

Your team is responsible for the following deliverables at the dates described above:

Project Proposal

A 2-page proposal describing what you plan to build. It must be specific enough that I can tell when you demonstrate your project that it meets the specs of the proposal. Include a budget for any supplies are not available in the stock. Describe the main subsystems of the design and the features of the PIC that you plan to use.

Status Report

A 4-page report (plus appendices) documenting your design at the midpoint. The status should include schematics of anything on a breadboard, block diagrams of the logic on your FPGA, and an outline of the routines used on the PIC. You should include as an appendix either your Verilog code or software that is mostly complete (but do not have to have both ready). You must be ready to demonstrate some working hardware in the lab.

Problem Presentations

Your team will sign up for a 15-minute presentation on one of four days near the end of the class. Your presentation should include a 3-minute overview of your project followed by in-depth presentation of a specific technical problem your team is working on and has not yet solved. The goal of the presentation is to get input from other students who might have ideas of how to solve your problem so you must explain the problem clearly enough to get meaningful suggestions back.

Project Demonstration

Demonstrate a working project to the instructor in the lab during your lab section. There will be signups for 30-minute demonstration periods, during which you will be asked technical questions about the operation of your design. Come prepared with printouts of your schematics, software and Verilog. If your project is one day late (Wednesday), one letter grade will be deducted. If your project is two days late (Thursday), two letter grades will be deducted. Teams unable to demonstrate at least some functional system by Thursday will fail the project.

Final Report

Turn in a final report documenting your design, not to exceed 12 pages plus appendices. Clearly explain how your design works. If you have developed techniques that would be useful for students in the future (i.e. how to interface to an LCD display), document these features very well so that future students may build on your work. The appendices should include complete schematics, code, and Verilog for your design.

Late projects will not be accepted except in the case of very unusual extenuating circumstances. Be careful to choose a project within a scope that you can reasonably expect to finish. If you realize your project is too large, contact me as soon as possible to renegotiate your project proposal. I will not accept revisions to the proposal after 12/1.

Grading

Your project will be graded as follows:

Proposal	10%
Status Report	20%
Presentation	10%
Demonstration	30%
Final Report	30%

If you feel there has been inequity between the work you and your teammate deliver, contact me personally.