DR. DAVID MONEY HARRIS

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Professional Interest: High-speed digital VLSI.
Microprocessor design, computer architecture, integer & floating point execution units, graphics, communications, networks, high speed circuits, embedded systems, security, wireless systems.

Education:

Stanford University **Stanford, CA**
Ph.D. March 1999. *Skew-Tolerant Domino Circuits* with Mark Horowitz.
GPA: 4.0 / 4.0

Massachusetts Institute of Technology **Cambridge, MA**
M. Eng. Degree in Electrical Engineering and Computer Science,
S. B. Degree in Electrical Engineering, S.B. Degree in Mathematics,
May 1994. **GPA: 5.0 / 5.0**

Experience:

Harvey Mudd College **Claremont, CA**
January 1999-Present. Associate Professor of Engineering.

One Hot Logic **Claremont, CA**
August 2001-Present. President. Founded a profitable startup manufacturing low-cost functional chip testers.

Sun Microsystems Labs **Mountain View, CA**
April 1997-Present. Visiting Professor. Research on low-overhead asynchronous applications of domino circuits with Turing award-winner Ivan Sutherland. Consulting one day per week. Multiple patents.

Boeing Corporation **Seattle, WA**
June-August 2005. Welliver Faculty Fellow.

Hewlett Packard **Fort Collins, CO**
May-August 2000. Consultant. Developed clock skew budgets and power grid analysis tools for Itanium 2 microprocessor. Taught circuit design seminars.

Evans & Sutherland **Salt Lake City, UT**
June-August 1999. Consultant. Architected OpenGL Geometry Engine delivering 44 Mvertices/s.

Intel Corporation **Santa Clara, CA**
June 1994-April 1997. Logic designer for Merced microprocessor; designed Integer Execution and Multimedia units, coded and tested several units. Circuit design on Pentium II & Itanium microprocessors. Trained junior logic and circuit designers. Multiple patents.
May-August 2004. Visiting Professor. Reconfigurable cryptographic Accelerators.

Design experience with Cadence, HSPICE, Verilog, Synopsys, Pathmill, FPGAs, and embedded microcontrollers. C, Perl, Java, etc.

Consulting experience with HAL Computer, Rockwell Semiconductor, TRW, Circuit Semantics, LightTime, Multigig.

Expert witness experience with Dechert in the VLSI / EDA field.

Honors & Activities: National Science Foundation fellow, winner of Microsoft Technical fellowship, Irwin Sizer Award for Most Significant Improvement to MIT Education, Putnam Exam honors, Tau Beta Pi member, 6.004 Computer Optimization Contest Winner, Secretary of Educational Studies Program, M. Eng. Thesis Prize recipient, President of Intel Newhire Network, founder and Chairperson of Stanford Educational Studies Program, Lyon's Award for Public Service, Commercial Pilot License, AngelFlight volunteer pilot.

Patents:

US Patent 6,769,007: Adder Circuit with a Regular Structure. July 27, 2004.
US Patent 6,710,436: Method and Apparatus for Electrostatically Aligning Integrated Circuits. March 23, 2004.
US Patent 6,580,303: Datapath Control Circuit with Adjustable Delay Elements. June 17, 2003.
US Patent 6,239,622: Self-timed Domino Circuit. May 29, 2001.
US Patent 6,169,422: Apparatus and Methods for High Throughput Self-Timed Domino Circuits. Jan 2, 2001.
US Patent 5,880,985: Efficient Combined Array for 2n bit n bit Multiplications. March 9, 1999.
US Patent 5,880,608: Pulsed Domino Latches. March 9, 1999.
US Patent 5,821,775: Interface Between Monotonic and Nonmonotonic Logic. October 13, 1998.
US Patent 5,517,136: Opportunistic Time-Borrowing Domino Logic. May 14, 1996.

Four other patents pending in the area of high-speed circuit/logic design.

Publications:

Kelley, Kyle, and Harris, David, "Very High Radix Scalable Montgomery Multipliers," *5th Intl. Workshop on System-on-Chip*, July 2005, pp. ***.

Harris, Sarah, and Harris, David, "Inexpensive Student-Assembled FPGA / Microcontroller Board," *Microelectronics Systems Education Conf.*, June 2005, pp. ***.

Harris, David, Krishnamurthy, Ram, Anders, Mark, Mathew, Sanu, and Hsu, Steven, "An Improved Unified Scalable Radix-2 Montgomery Multiplier," *IEEE Symposium on Computer Arithmetic*, June 20005, pp. ***.

Shultz, Kim, Chiprout, Eli, Harris, David, Grover, Shamit, Quach, Quan, Locascio, Mark, and Kelley, Kyle, "Early dynamic power grid robustness testing using a torus," submitted to *Great Lakes Symposium on VLSI* (2005).

Harris, David, "Logical Effort of Higher Valency Adders," *Asilomar Conf. Signals, Systems, and Computers*, Nov. 2004, pp. 1358-1362.

Linderman, Michael, Harris, David, and Diaz, David, "Bounding Bus Delay and Noise Effects of On-Chip Inductance," *IEEE Workshop on Signal Propagation on Interconnects*, April 2004.

Weste, Neil, and Harris, David, *CMOS VLSI Design: A Circuits and Systems Perspective*, Addison Wesley, May 2004.

Harris, David, "An Exponentiation Unit for an OpenGL Lighting Engine," *IEEE Trans. Computers*, vol. 53, no. 3, March 2004, pp. 251-258.

Harris, David, "A Taxonomy of Prefix Networks," *Asilomar Conf. Signals, Systems, and Computers*, Nov. 2003, pp. 2213-2217.

Harris, David, and Sutherland, Ivan, "Logical Effort of Prefix Adders," *Asilomar Conf. Signals, Systems, and Computers*, Nov. 2003, pp. 673-678.

Harris, David, and Akin, Tayfun, "A Cross-Cultural Chip Design Project," *Proc. American Society of Engineering Educators Annual Conf.,* June 2003.

Harris, David, and Diaz, David, "TestosterICs: A Low-Cost Functional Chip Tester," *Microelectronics Systems Education Conf*., June 2003.

Harris, David, Breed, Genevive, Erler, Matthew, and Diaz, David, "Comparison of Noise Tolerant Precharge (NTP) to Conventional Feedback Keepers for Dynamic Logic," *Great Lakes Symposium on VLSI*, April 2003.

Harris, David, "The Microprocessor as a Microcosm: A Hands-on Approach to VLSI Design Education," *ASEE/IEEE Frontiers in Education Conf.*, November 2002.

Harris, David, "A Freshman Advising Seminar on Digital Electronics and Chip Design," *Proc. American Society of Engineering Educators Annual Conf.*, June 2002.

Harris, David, and Naffziger, Sam, "Statistical Clock Skew Modeling with Data Delay Variations," *IEEE Trans. VLSI Systems*, vol. 9, no. 6, December 2001, pp. 888-898.

Harris, David, "A Powering Unit for an OpenGL Lighting Engine," *Proc. Asilomar Conf. on Signals, Systems, and Computers*, November

2001. (invited paper)

Harris, David, "A Case for Project-Based Design Education," *Intl. J. Engineering Education*, vol. 17, no 4-5, pp. 367-369, 2001.

Harris, David, "Skew-Tolerant Domino Circuits," *Tech-Online Online Symposium for Electronics Engineers*, Fall 2000. www.techonline.com

Harris, David, *Skew-Tolerant Circuit Design*, Morgan Kaufmann Publishers, May 2000.

Harris, David, Horowitz, Mark, and Liu, Dean, "Timing Analysis Including Clock Skew," *IEEE Trans. Computer-Aided Design*, November 1999, pp. 1608-1618.

Harris, David, "A Case for Project-Based Design Education," *Proc. Mudd Design Workshop II*, Claremont, CA, May 1999.

Coats, Bill, *et al*., "A Counterflow pipeline experiment," *Proc. Fifth Intl. Conf. Asynchronous Circuits and Systems*, Barcelona, Spain, April 1999, pp. 161-172.

Harris, David, Horowitz, Mark, and Liu, Dean, "Timing Analysis Including Clock Skew," *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, Monterey, CA, March 1999, pp. 15-20.

Sutherland, Ivan, Sproull, Bob, and Harris, David, *Logical Effort: Designing Fast CMOS Circuits*, Morgan Kaufmann Publishers, 1999.

Harris, David, and Horowitz, Mark, "Skew-Tolerant Domino Circuits," *IEEE J. Solid-State Circuits*, Nov. 1997, pp. 1702-1711.

Harris, David, Oberman, Stuart, and Horowitz, Mark, "SRT Division Algorithms and Architectures," *Proc. 13th IEEE Symposium on Computer Arithmetic*, July 1997.

Harris, David, and Horowitz, Mark, "Skew-Tolerant Domino Circuits," *ISSCC Dig. Tech Papers*, Feb. 1997, pages 422-423.

Dally, W., Dennison, L., Harris, D., Kan, K., and Xanthopoulos, T., "The Reliable Router: A Reliable and High-Performance Communication Substrate for Computers," *Lecture Notes in Computer Science, Vol. 853, Proc. First Intl. Workshop on Parallel Computer Routing and Communication*, pp. 241-255, 1994.

Dally, W., Dennison, L., Harris, D., Kan, K., and Xanthopoulos, T., "Architecture and implementation of the reliable router," *Hot Interconnects II*, 1994.

Barbieri, Harris, & Eeckman, "A Simulation of Neural Processing in the Auditory Path of the Barn Owl," in Eeckman (ed) *Computation in Neurons and Neural Systems*; Kluwer Academic Publishers, 1994.

Harris, David, and Harris, Daniel "A Low-Cost pH Meter for the Classroom," *J. Chem. Educ*. 1992, Volume 69, page 563.

Harris, David "A Taxonomy of Ceiling Tile," *J. Irreproducible Results*, 1992, Volume 37, Number 3, page 7-8.

Invited Talks

David Evans Conf. Computer Eng. 2005 CMOS VLSI Design
DATE 2004 Advanced Domino Circuit Design Tutorial
ASPDAC 2003 High-Speed CMOS Circuit Design Tutorial
ISSCC 2002 Microprocessor Design Workshop
ISSCC 2001 Logical Effort Tutorial
ISSCC 2001 Panel Session on Taming the Microprocessor Monster
ISSCC 2000 Workshop on High Speed Microprocessor Design

Teaching Experience:

E155: Microprocessor Applications
Harvey Mudd College Fall 2004, 2003, 2002, 2000, 1999
E151: Engineering Electronics
Harvey Mudd College Fall 2001
E59: Introduction to Systems Engineering
Harvey Mudd College Fall 2004, 2002, 2001
E158: Introduction to CMOS VLSI Design
Harvey Mudd College Spring 2005, 2004, 2003, 2002, 2001
FYS1: Digital Electronics & Chip Design for Freshmen
Harvey Mudd College Fall 2003, Fall 2002, 2001, 2000, 1999
E85: Introduction to Computer Engineering
Harvey Mudd College Spring 2001, 2000, 1999
E101: Advanced Systems Engineering
Harvey Mudd College Fall 2003
Engineering Clinic
Harvey Mudd College
Intel Corporation Power Grid Analysis 2003
Sandia National Labs FT Ion Mobility Spectrometer 2003, 2002
Qualcomm GPS Data Recorder 2002
Aerospace Corporation Bit Error Rate Tester 2001, A/D 2004
Texas Instruments GPS Searcher 2000, 2001
Opto22 I/O Controller 2000
Sun Microsystems Chip Tester 1998, 1999
Evans & Sutherland Geometry Engine 1999
Sierra Wireless USB / Ethernet Bridge 2004
High Speed CMOS VLSI Design
Industrial courses taught at:
Sun Microsystems Winter 2004
Qualcomm Summer 2003
Evans & Sutherland Summer 1999
Intel Corporation Fall 1998
Intel Corporation Spring 1998

UC Berkeley Extension Winter 1998
HAL Computer Fall 1997

EE371: Advanced VLSI Circuit Design
Teaching Fellow (co-taught with Professor M. Horowitz): Stanford 1996

Digital Electronics & Chip Design (for high school students)
Educational Studies Program: Stanford 1996-1998

EE271: Introduction to VLSI Design
Teaching Assistant for Professor M. Horowitz: Stanford 1995

Advanced VLSI Design (intensive course at Cray Computer)
Teaching Assistant for Professor W. Dally: 1994

6.090: "VLSI for Freshmen and Sophomores:" master's thesis project
Instructor (co-taught with Professor W. Dally): MIT 1994

6A27: Introduction to Digital Electronics (freshman seminar)
Instructor: MIT 1993-1994

18.06: Linear Algebra & 18:03: Differential Equations
Tutor: MIT Experimental Study Group 1991-1994

Academic Leadership:

Director, Engineering Computational Facility 2001-
Chair, Engineering Faculty Search Committee 2001, 2004-05
Chair, Engineering Petitions Committee, 2000-01, 2003
Chair, Scholarly Standing Committee, 2004-05