HW 10; Due December 4th

E85 – Fall 2015

Please turn in 2 parts: A, and B as separated documents (stapled or paper clipped etc.). Put your name on all pages.

Part A (50%):

7.7, 7.11, 7.23, 7.28, 7.39

Part B (50%):

1) Interview question 7.2:

If additional pipeline stages allow a processor to go faster, why don’t processors have 100 pipeline stages? Explain clearly and concisely, while addressing the costs/benefits of adding stages to a pipelined CPU.

2) Go on digikey.com and locate a Cortex M7 microcontroller from ST Microelectronics that is available in a 100 pin LQFP package. Choose the lowest cost part.

What is the Part Number?

How much RAM does it have (in kB)? How much flash memory does it have (in kB)?

Open the datasheet. Find the memory map.

At what address does APB1 start?

At what address is GPIOA (GPIOx is the same as PORT from the example in class).

PORT was at 0x41004400 for the M0+ chip in class. What is at this address for this processor?

3) Using the data sheet from the Cortex M0+ discussed in class (http://www.atmel.com/Images/Atmel-42363-SAM-D11_Datasheet.pdf)

Based on the product dependences (26.5) for the SPI peripheral, what items must be configured before the SPI can be used?

Suppose you want to turn on (enable) the SPI peripheral as a master with: MSB transferred first, CPOL = 1, CPHA = 1, a standard SPI frame, PAD[0] used for data out, PAD[1] used for slave_SS, PAD[2] used for data in, PAD[3] used for SCK. Have the SPI off when it standby, have IBON = 0. Setting reserve bits to 0.

What is the address of CTRLA?

Write a single line of C that sets the value of CTRLA to the required value.

Survey:

How much time did you spend on this assignment?