HW 6; Due October 28th

E85 – Fall 2015

Please turn in 2 parts: A, and B as separated documents (stapled or paper clipped etc.). Put your name on all pages.

Part A (35%):

5.2, 5.16

Part B (35%):

5.22, 5.47

Part C (30%):

You have to collect data rapidly from an analog to digital converter (ADC) and do some data processing on it. You decide you will use an FPGA for this task. The ADC uses a 100 MHz clock (CLK) and delivers 16-bit data once per clock cycle to the FPGA on 16 wires (DAT => DAT0-DAT15). You want to capture at most 1024 samples of data at a time. You want to take data whenever the system is enable (EN).

You have 65536 bits of memory available with up to 1 write port and 1 read ports of any width. The write port is enabled by a pin WE. You may also have up to 64 DFF for your design (I doubt you need this many).

Design a system that allows you to store 4 datasets into the memory for retrieval by the data processing module. Design any FSM diagrams you might need. Show a schematic at least in block diagram form of what your solution is. Write Verilog that implements your design.

(Hint: you may find the RAM example helpful in solving this problem, p. 272 of the ARM edition).

Survey:

How much time did you spend on this assignment?